

TITLE	Page
Cover Sheet	1
Block Diagram	2
CPU-CLK/Control/MISC/PEG/Memory	3,4,5,6,7
CPU-Power,CPU-GND	8,9
OC socket	10
DDRIV X8	11,12,13,14,15,16
PCH-LPC/HDA/RTC/MISC/SPI	17
PCH-DMI/PCIE/USB/SATA	18
PCH-CLK/GPIO	19
PCH-POWER/GND	20,21
PCH Strap	22
CLK GEN-IDT49325	23
CLK BUFFER831/MCU812	24
CPU PCIE SWITCH	25
PCIESLOT	26,27,28,29,30
SIO-NTC6779D/PS2	31,32
FAN CONTROLLOR	33,34,35,36
Dual BIOS	37
Audio Codec ALC1150	38,39
LAN INTEL i219V	40
ASM1142 RUSB3.1 2PORT	41
ASM1142 FRUSB3.1 1PORT	42
Front USB3.1 switch	43
VL805-USB30-4PORT	44
USB HOTKEY F75504	45
SLG55593A	46
GPIO CONTROLLER	47
PCIE& SATA Redriver	48
M.2 CONNECTOR	49
U.2 CONNECTOR	50
SATA Connector	51
WIFI +BTconnector	52
USB3.0 Connector	53
USB3.1 REAR TYPE-A+C CONN	54
USB3.0 FRONT TYPE-C CONN	55
Rear/Front USB2.0	56
FRONT USB REDRIVER CONNECTOR	57
ACPI controller UPI	58
CPU Power-ISL6388	59
CPU Power -ISL6617	60
VCOR FCH5823 PHASE 1~8	61
VCOR FCH5823 PHASE 9~12	62
DDR Power-VPP25	63
DDR Power1-PV3203-2-Phase	64
DDR Power2-PV3203-2-Phase	65
PCH Power -PV3203Q-1Phase	66
VTTDDR&VREF&VCCIO	67
CURRENT and VOLTAGE SENSE	68
ATX F_Panel/EMI/TPM	69
LED STRIP CONTROL	70
BOTTON	71
DEBUG LED & JLED	72
Manual Parts	73
Power Map	74
GPIO MAP	75
Power Sequence	76
Revision History	77

MS-7A21

ATX

Ver: 11

Haswell-E Platform

CPU:

System Chipset:

Haswell-E

Wellsburg

Onboard Chip:

HD Audio Codec:ALC1150

LAN-INTEL LAN i219

SIO:NTC6792D

Dual Flash ROM: SPI 64 MB X2

Main Memory:

DDRIV (1666MHz) * 8 (Dual Channel)

ACPI:

PWM:

UPI

VRD12.5 -ISL 6388

Expansion Slots:

Other:

PCI Express (X16) Slot * 4

PCI Express (X8) Slot * 1

PCI Express (X1) Slot * 1

SATA-EX *1

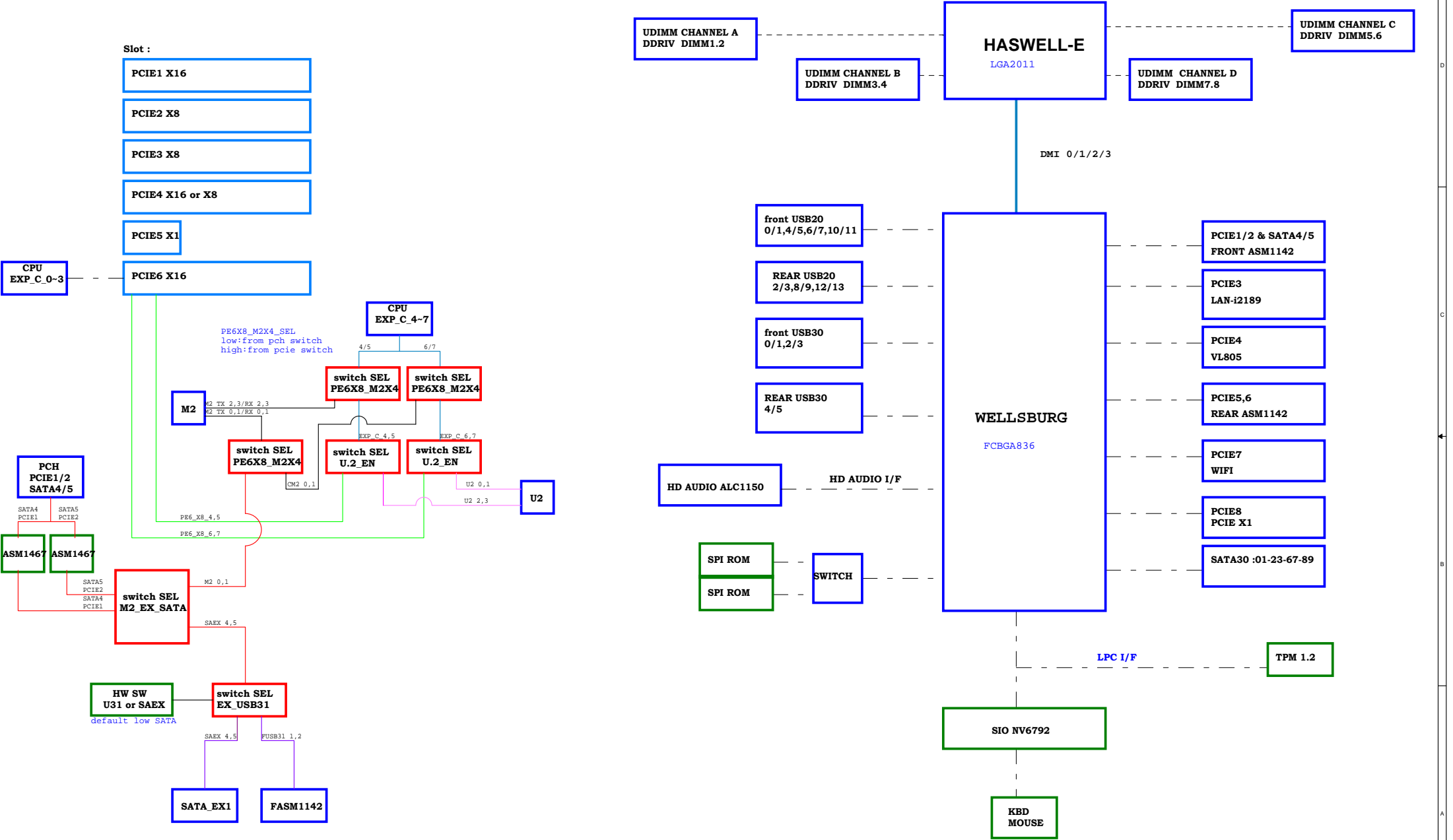
SATA3.0 *6

REAR USB2.0 x11

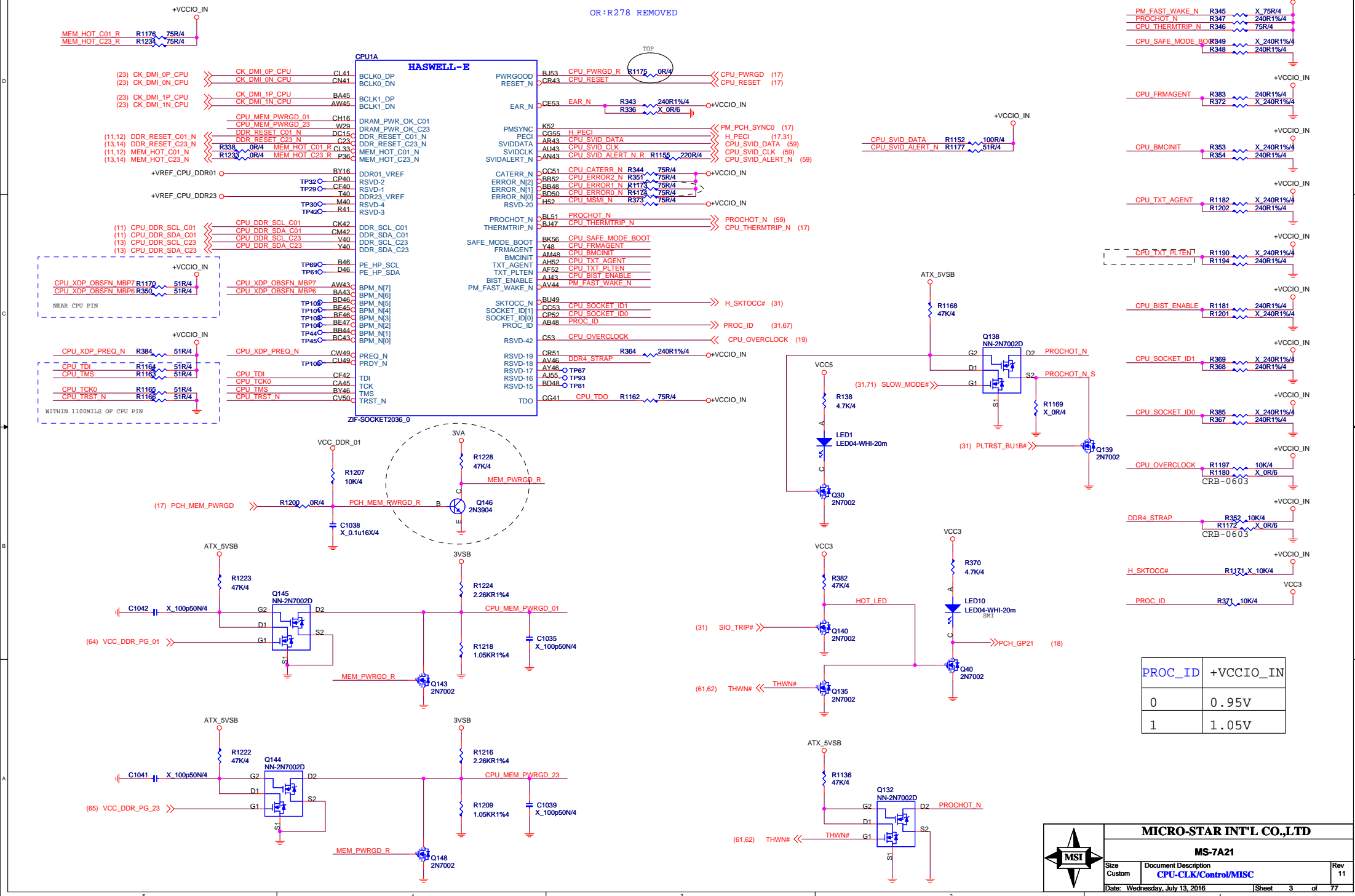
REAR USB3.0 x6 + USB3.1 x2

FRONT USB3.0 x4 + USB3.1 x1

MS-7A21 Block Diagram



CPU-CLK/Control/MISC



CPU-DMI / PEG

CPU1F

HASWELL-E

(18) DMI_RX3	DMI_RX3#	C370	0.1u10X4 DMI CPU RX3	E47	DMI_RX_DP[3]	D42	DMI_CPU_TX3	C343	0.1u10X4 DMI TX3	>>>	DMI_TX3	(18)
(18) DMI_RX2	DMI_RX2#	C345	0.1u10X4 DMI CPU RX2	D48	DMI_RX_DP[2]	E43	DMI_CPU_TX2	C355	0.1u10X4 DMI TX2	>>>	DMI_TX2	(18)
(18) DMI_RX1	DMI_RX1#	C381	0.1u10X4 DMI CPU RX1	E49	DMI_RX_DP[1]	D44	DMI_CPU_TX1	C348	0.1u10X4 DMI TX1	>>>	DMI_TX1	(18)
(18) DMI_RX0	DMI_RX0#	C369	0.1u10X4 DMI CPU RX0	D50	DMI_RX_DP[0]	E45	DMI_CPU_TX0	C341	0.1u10X4 DMI TX0	>>>	DMI_TX0	(18)
(18) DMI_RX3#	DMI_RX3#	C363	0.1u10X4 DMI CPU RX3#	C47	DMI_RX_DN[3]	B42	DMI_CPU_TX3#	C344	0.1u10X4 DMI TX3#	>>>	DMI_TX3#	(18)
(18) DMI_RX2#	DMI_RX2#	C346	0.1u10X4 DMI CPU RX2#	B48	DMI_RX_DN[2]	C43	DMI_CPU_TX2#	C356	0.1u10X4 DMI TX2#	>>>	DMI_TX2#	(18)
(18) DMI_RX1#	DMI_RX1#	C374	0.1u10X4 DMI CPU RX1#	C49	DMI_RX_DN[1]	B44	DMI_CPU_TX1#	C342	0.1u10X4 DMI TX1#	>>>	DMI_TX1#	(18)
(18) DMI_RX0#	DMI_RX0#	C362	0.1u10X4 DMI CPU RX0#	B50	DMI_RX_DN[0]	C45	DMI_CPU_TX0#	C347	0.1u10X4 DMI TX0#	>>>	DMI_TX0#	(18)
(30) EXP_C_RXP_7				M56	PE1B_RX_DP[7]	L49				>>>	EXP_C_TXP_7	(30)
(30) EXP_C_RXP_6				L57	PE1B_RX_DP[6]	K48				>>>	EXP_C_TXP_6	(30)
(30) EXP_C_RXP_5				M54	PE1B_RX_DP[5]	L47				>>>	EXP_C_TXP_5	(30)
(30) EXP_C_RXP_4				L53	PE1B_RX_DP[4]	K46				>>>	EXP_C_TXP_4	(30)
(30) EXP_C_RXN_7				K56	PE1B_RX_DN[7]	J49				>>>	EXP_C_TXN_7	(30)
(30) EXP_C_RXN_6				J57	PE1B_RX_DN[6]	H48				>>>	EXP_C_TXN_6	(30)
(30) EXP_C_RXN_5				K54	PE1B_RX_DN[5]	J47				>>>	EXP_C_TXN_5	(30)
(30) EXP_C_RXN_4				J53	PE1B_RX_DN[4]	H46				>>>	EXP_C_TXN_4	(30)
(30) EXP_C_RXP_3				G58	PE1A_RX_DP[3]	L45				>>>	EXP_C_TXP_3	(30)
(30) EXP_C_RXP_2				F54	PE1A_RX_DP[2]	K44				>>>	EXP_C_TXP_2	(30)
(30) EXP_C_RXP_1				F52	PE1A_RX_DP[1]	L43				>>>	EXP_C_TXP_1	(30)
(30) EXP_C_RXP_0				E51	PE1A_RX_DP[0]	K42				>>>	EXP_C_TXP_0	(30)
(30) EXP_C_RXN_3				E55	PE1A_RX_DN[3]	J45				>>>	EXP_C_TXN_3	(30)
(30) EXP_C_RXN_2				D54	PE1A_RX_DN[2]	H44				>>>	EXP_C_TXN_2	(30)
(30) EXP_C_RXN_1				D52	PE1A_RX_DN[1]	J43				>>>	EXP_C_TXN_1	(30)
(30) EXP_C_RXN_0				C51	PE1A_RX_DN[0]	H42				>>>	EXP_C_TXN_0	(30)
Not functional in HSW-E 28-lane SKU						Not functional in HSW-E 28-lane SKU						
(28) EXP_A_RXP_15				BB56	PE2D_RX_DP[15]	BA47				>>>	EXP_A_TXP_15	(28)
(28) EXP_A_RXP_14				BA57	PE2D_RX_DP[14]	AY48				>>>	EXP_A_TXP_14	(28)
(28) EXP_A_RXP_13				AT58	PE2D_RX_DP[13]	BA49				>>>	EXP_A_TXP_13	(28)
(28) EXP_A_RXP_12				AV58	PE2D_RX_DP[12]	AY50				>>>	EXP_A_TXP_12	(28)
(28) EXP_A_RXN_15				AY56	PE2D_RX_DN[15]	AW47				>>>	EXP_A_TXN_15	(28)
(28) EXP_A_RXN_14				AY58	PE2D_RX_DN[14]	AV48				>>>	EXP_A_TXN_14	(28)
(28) EXP_A_RXN_13				AP58	PE2D_RX_DN[13]	AW49				>>>	EXP_A_TXN_13	(28)
(28) EXP_A_RXN_12				AT58	PE2D_RX_DN[12]	AV50				>>>	EXP_A_TXN_12	(28)
(28) EXP_A_RXP_11				AU57	PE2C_RX_DP[11]	BA51				>>>	EXP_A_TXP_11	(28)
(28) EXP_A_RXP_10				AL57	PE2C_RX_DP[10]	BB54				>>>	EXP_A_TXP_10	(28)
(28) EXP_A_RXP_9				AM58	PE2C_RX_DP[9]	BA53				>>>	EXP_A_TXP_9	(28)
(28) EXP_A_RXP_8				AK56	PE2C_RX_DP[8]	AY52				>>>	EXP_A_TXP_8	(28)
(28) EXP_A_RXN_11				AR57	PE2C_RX_DN[11]	AW51				>>>	EXP_A_TXN_11	(28)
(28) EXP_A_RXN_10				AJ57	PE2C_RX_DN[10]	AY54				>>>	EXP_A_TXN_10	(28)
(28) EXP_A_RXN_9				AK58	PE2C_RX_DN[9]	AW53				>>>	EXP_A_TXN_9	(28)
(28) EXP_A_RXN_8				AH56	PE2C_RX_DN[8]	AV52				>>>	EXP_A_TXN_8	(28)
(28) EXP_A_RXP_7				AF58	PE2B_RX_DP[7]	AT54				>>>	EXP_A_TXP_7	(28)
(28) EXP_A_RXP_6				AE58	PE2B_RX_DP[6]	AR53				>>>	EXP_A_TXP_6	(28)
(28) EXP_A_RXP_5				AD56	PE2B_RX_DP[5]	AK54				>>>	EXP_A_TXP_5	(28)
(28) EXP_A_RXP_4				AD54	PE2B_RX_DP[4]	AJ53				>>>	EXP_A_TXP_4	(28)
(28) EXP_A_RXN_7				AE57	PE2B_RX_DN[7]	AP54				>>>	EXP_A_TXN_7	(28)
(28) EXP_A_RXN_6				AC55	PE2B_RX_DN[6]	AN53				>>>	EXP_A_TXN_6	(28)
(28) EXP_A_RXN_5				AB56	PE2B_RX_DN[5]	AH54				>>>	EXP_A_TXN_5	(28)
(28) EXP_A_RXN_4				AB54	PE2B_RX_DN[4]	AG53				>>>	EXP_A_TXN_4	(28)
(28) EXP_A_RXP_3				W55	PE2A_RX_DP[3]	AP52				>>>	EXP_A_TXP_3	(28)
(28) EXP_A_RXP_2				V56	PE2A_RX_DP[2]	AR51				>>>	EXP_A_TXP_2	(28)
(28) EXP_A_RXP_1				V54	PE2A_RX_DP[1]	AP50				>>>	EXP_A_TXP_1	(28)
(28) EXP_A_RXP_0				N55	PE2A_RX_DP[0]	AR49				>>>	EXP_A_TXP_0	(28)
(28) EXP_A_RXN_3				U55	PE2A_RX_DN[3]	AM52				>>>	EXP_A_TXN_3	(28)
(28) EXP_A_RXN_2				T56	PE2A_RX_DN[2]	AN51				>>>	EXP_A_TXN_2	(28)
(28) EXP_A_RXN_1				T54	PE2A_RX_DN[1]	AM50				>>>	EXP_A_TXN_1	(28)
(28) EXP_A_RXN_0				L55	PE2A_RX_DN[0]	AN49				>>>	EXP_A_TXN_0	(28)

ZIF-SOCKET2036_0

CPU1G

HASWELL-E

(26) EXP_B_RXP_15				AR45	PE3D_RX_DP[15]	P44				>>>	EXP_B_TXP_15	(26)
(26) EXP_B_RXP_14				AP46	PE3D_RX_DP[14]	AA43				>>>	EXP_B_TXP_14	(26)
(26) EXP_B_RXP_13				AR47	PE3D_RX_DP[13]	AB44				>>>	EXP_B_TXP_13	(26)
(26) EXP_B_RXP_12				AJ47	PE3D_RX_DP[12]	AC45				>>>	EXP_B_TXP_12	(26)
(26) EXP_B_RXN_15				AN45	PE3D_RX_DN[15]	T44				>>>	EXP_B_TXN_15	(26)
(26) EXP_B_RXN_14				AM46	PE3D_RX_DN[14]	AC43				>>>	EXP_B_TXN_14	(26)
(26) EXP_B_RXN_13				AN47	PE3D_RX_DN[13]	Y44				>>>	EXP_B_TXN_13	(26)
(26) EXP_B_RXN_12				AG47	PE3D_RX_DN[12]	AA45				>>>	EXP_B_TXN_12	(26)
(26) EXP_B_RXP_11				AJ49	PE3C_RX_DP[11]	AB46				>>>	EXP_B_TXP_11	(26)
(26) EXP_B_RXP_10				AH50	PE3C_RX_DP[10]	AC47				>>>	EXP_B_TXP_10	(26)
(26) EXP_B_RXP_9				AJ51	PE3C_RX_DP[9]	U45				>>>	EXP_B_TXP_9	(26)
(26) EXP_B_RXP_8				AH48	PE3C_RX_DP[8]	T46				>>>	EXP_B_TXP_8	(26)
(26) EXP_B_RXN_11				AG49	PE3C_RX_DN[11]	Y46				>>>	EXP_B_TXN_11	(26)
(26) EXP_B_RXN_10				AF50	PE3C_RX_DN[10]	AA47				>>>	EXP_B_TXN_10	(26)
(26) EXP_B_RXN_9				AG51	PE3C_RX_DN[9]	R45				>>>	EXP_B_TXN_9	(26)
(26) EXP_B_RXN_8				AF48	PE3C_RX_DN[8]	P46				>>>	EXP_B_TXN_8	(26)
(25) EXP_B_RXP_7				AC51	PE3B_RX_DP[7]	U49				>>>	EXP_B_TXP_7	(25)
(25) EXP_B_RXP_6				AC53	PE3B_RX_DP[6]	T50				>>>	EXP_B_TXP_6	(25)
(25) EXP_B_RXP_5				AB52	PE3B_RX_DP[5]	U51				>>>	EXP_B_TXP_5	(25)
(25) EXP_B_RXP_4				AB50	PE3B_RX_DP[4]	T52				>>>	EXP_B_TXP_4	(25)
(25) EXP_B_RXN_7				AA51	PE3B_RX_DN[7]	R49				>>>	EXP_B_TXN_7	(25)
(25) EXP_B_RXN_6				AA53	PE3B_RX_DN[6]	P50				>>>	EXP_B_TXN_6	(25)
(25) EXP_B_RXN_5				Y52	PE3B_RX_DN[5]	R51				>>>	EXP_B_TXN_5	(25)
(25) EXP_B_RXN_4				Y50	PE3B_RX_DN[4]	P52				>>>	EXP_B_TXN_4	(25)
(25) EXP_B_RXP_3				AC49	PE3A_RX_DP[3]	T48				>>>	EXP_B_TXP_3	(25)
(25) EXP_B_RXP_2				AH48	PE3A_RX_DP[2]	U47				>>>	EXP_B_TXP_2	(25)
(25) EXP_B_RXP_1				AJ45	PE3A_RX_DP[1]	L51				>>>	EXP_B_TXP_1	(25)
(25) EXP_B_RXP_0				AH44	PE3A_RX_DP[0]	K50				>>>	EXP_B_TXP_0	(25)
(25) EXP_B_RXN_3				AF49	PE3A_RX_DN[3]	P48				>>>	EXP_B_TXN_3	(25)
(25) EXP_B_RXN_2				AG45	PE3A_RX_DN[2]	R47				>>>	EXP_B_TXN_2	(25)
(25) EXP_B_RXN_1				AF44	PE3A_RX_DN[1]	J51				>>>	EXP_B_TXN_1	(25)
(25) EXP_B_RXN_0					PE3A_RX_DN[0]	H50				>>>	EXP_B_TXN_0	(25)

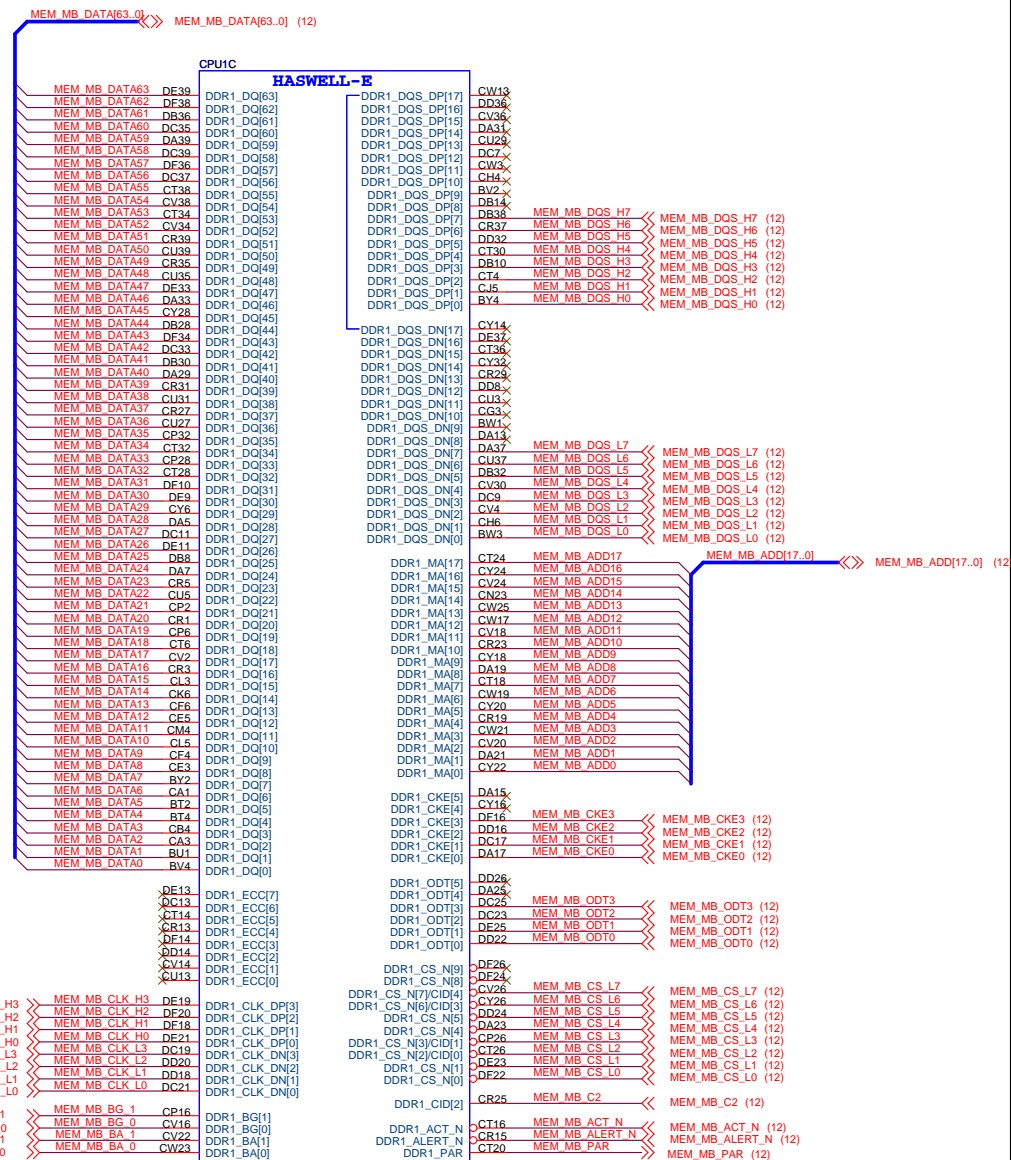
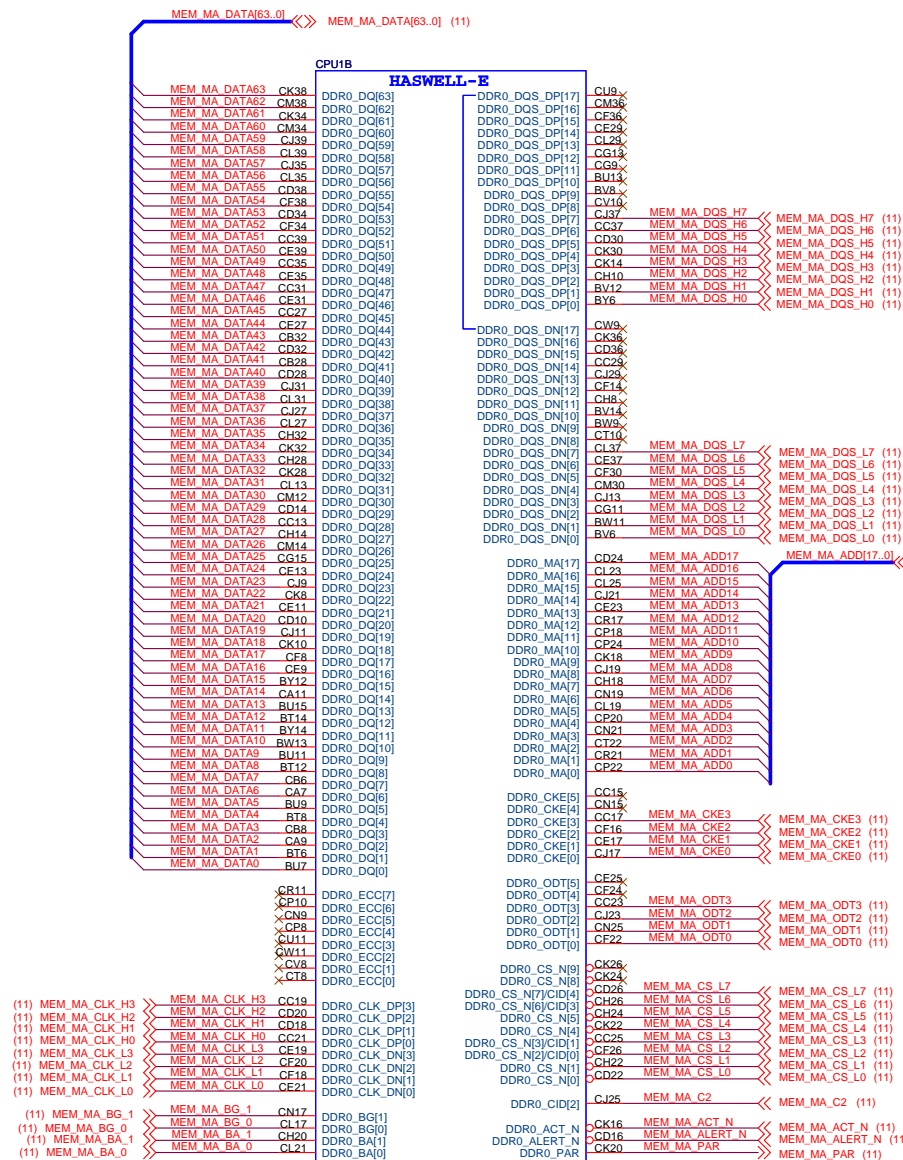
ZIF-SOCKET2036_0



MICRO-STAR INT'L CO.,LTD

MS-7A21

Size	Document Description	Rev
Custom	CPU-DMI/PEG	11
Date: Wednesday, July 13, 2016	Sheet 4 of 77	



CPU-Memory2/3

MEM_MC_DATA[63..0] >>> MEM_MC_DATA[63..0] (13)

CPU1D

HASWELL-E

MEM_MC_DATA63 AL7
MEM_MC_DATA62 AK8
MEM_MC_DATA61 AE9
MEM_MC_DATA60 AL9
MEM_MC_DATA59 AL9
MEM_MC_DATA58 AK10
MEM_MC_DATA57 AG7
MEM_MC_DATA56 AG9
MEM_MC_DATA55 AL15
MEM_MC_DATA54 AK14
MEM_MC_DATA53 AF14
MEM_MC_DATA52 AG15
MEM_MC_DATA51 AL13
MEM_MC_DATA50 AK12
MEM_MC_DATA49 AE12
MEM_MC_DATA48 AE11
MEM_MC_DATA47 Y8
MEM_MC_DATA46 AA8
MEM_MC_DATA45 L11
MEM_MC_DATA44 L10
MEM_MC_DATA43 AB8
MEM_MC_DATA42 AA11
MEM_MC_DATA41 W11
MEM_MC_DATA40 U9
MEM_MC_DATA39 M6
MEM_MC_DATA38 K6
MEM_MC_DATA37 L9
MEM_MC_DATA36 J9
MEM_MC_DATA35 P6
MEM_MC_DATA34 R7
MEM_MC_DATA33 K8
MEM_MC_DATA32 T24
MEM_MC_DATA31 T24
MEM_MC_DATA30 V24
MEM_MC_DATA29 T28
MEM_MC_DATA28 V28
MEM_MC_DATA27 R23
MEM_MC_DATA26 U23
MEM_MC_DATA25 R27
MEM_MC_DATA24 U27
MEM_MC_DATA23 AC51
MEM_MC_DATA22 AE31
MEM_MC_DATA21 AA35
MEM_MC_DATA20 AC35
MEM_MC_DATA19 AB30
MEM_MC_DATA18 AB30
MEM_MC_DATA17 AB34
MEM_MC_DATA16 AD34
MEM_MC_DATA15 W34
MEM_MC_DATA14 T32
MEM_MC_DATA13 R35
MEM_MC_DATA12 U35
MEM_MC_DATA11 V30
MEM_MC_DATA10 V30
MEM_MC_DATA9 U33
MEM_MC_DATA8 V34
MEM_MC_DATA7 U37
MEM_MC_DATA6 T38
MEM_MC_DATA5 AC39
MEM_MC_DATA4 AE37
MEM_MC_DATA3 Y38
MEM_MC_DATA2 R37
MEM_MC_DATA1 AB38
MEM_MC_DATA0 AD38

DDR2_DQS_DP[17] AD26
DDR2_DQS_DP[16] AH10
DDR2_DQS_DP[15] AH19
DDR2_DQS_DP[14] V8
DDR2_DQS_DP[13] V26
DDR2_DQS_DP[12] AC33
DDR2_DQS_DP[11] T34
DDR2_DQS_DP[10] AB38
DDR2_DQS_DP[9] AC29
DDR2_DQS_DP[8] AJ7
DDR2_DQS_DP[7] AH12
DDR2_DQS_DP[6] AB10
DDR2_DQS_DP[5] N7
DDR2_DQS_DP[4] U25
DDR2_DQS_DP[3] AB32
DDR2_DQS_DP[2] U31
DDR2_DQS_DP[1] V38
DDR2_DQS_DP[0] V38

MEM_MC_DQS_H7 <<< MEM_MC_DQS_H7 (13)
MEM_MC_DQS_H6 <<< MEM_MC_DQS_H6 (13)
MEM_MC_DQS_H5 <<< MEM_MC_DQS_H5 (13)
MEM_MC_DQS_H4 <<< MEM_MC_DQS_H4 (13)
MEM_MC_DQS_H3 <<< MEM_MC_DQS_H3 (13)
MEM_MC_DQS_H2 <<< MEM_MC_DQS_H2 (13)
MEM_MC_DQS_H1 <<< MEM_MC_DQS_H1 (13)
MEM_MC_DQS_H0 <<< MEM_MC_DQS_H0 (13)

MEM_MC_ADD[17..0] >>> MEM_MC_ADD[17..0] (13)

DDR2_MA[17] T14
DDR2_MA[16] P14
DDR2_MA[15] R13
DDR2_MA[14] Y14
DDR2_MA[13] P12
DDR2_MA[12] W21
DDR2_MA[11] AA15
DDR2_MA[10] P20
DDR2_MA[9] L19
DDR2_MA[8] U19
DDR2_MA[7] M18
DDR2_MA[6] P18
DDR2_MA[5] R19
DDR2_MA[4] L17
DDR2_MA[3] T18
DDR2_MA[2] M16
DDR2_MA[1] L15
DDR2_MA[0] L15

DDR2_CKE[5] AD22
DDR2_CKE[4] AB22
DDR2_CKE[3] Y22
DDR2_CKE[2] T22
DDR2_CKE[1] U21
DDR2_CKE[0] R21

DDR2_ODT[5] AD14
DDR2_ODT[4] AE14
DDR2_ODT[3] AB14
DDR2_ODT[2] R15
DDR2_ODT[1] W15
DDR2_ODT[0] Y16

DDR2_CS_N[9] AD16
DDR2_CS_N[8] AD16
DDR2_CS_N[7] CID[4]
DDR2_CS_N[6] CID[3]
DDR2_CS_N[5] CID[2]
DDR2_CS_N[4] CID[1]
DDR2_CS_N[3] CID[0]
DDR2_CS_N[2] CID[0]
DDR2_CS_N[1] CID[0]
DDR2_CS_N[0] CID[0]

DDR2_BG[1] AD20
DDR2_BG[0] AD21
DDR2_ACT_N M14
DDR2_PAR M14

MEM_MD_DATA[63..0] >>> MEM_MD_DATA[63..0] (14)

CPU1E

HASWELL-E

MEM_MD_DATA63 AB6
MEM_MD_DATA62 AC3
MEM_MD_DATA61 V6
MEM_MD_DATA60 AE4
MEM_MD_DATA59 AE4
MEM_MD_DATA58 AC5
MEM_MD_DATA57 W3
MEM_MD_DATA56 V4
MEM_MD_DATA55 AL1
MEM_MD_DATA54 AL3
MEM_MD_DATA53 AE3
MEM_MD_DATA52 AG5
MEM_MD_DATA51 AL5
MEM_MD_DATA50 AG1
MEM_MD_DATA49 AG1
MEM_MD_DATA48 AG3
MEM_MD_DATA47 G7
MEM_MD_DATA46 D6
MEM_MD_DATA45 A9
MEM_MD_DATA44 C9
MEM_MD_DATA43 F6
MEM_MD_DATA42 E5
MEM_MD_DATA41 F8
MEM_MD_DATA40 E9
MEM_MD_DATA39 R3
MEM_MD_DATA38 K2
MEM_MD_DATA37 N3
MEM_MD_DATA36 P4
MEM_MD_DATA35 L1
MEM_MD_DATA34 J1
MEM_MD_DATA33 H4
MEM_MD_DATA32 B24
MEM_MD_DATA31 B24
MEM_MD_DATA30 C25
MEM_MD_DATA29 E29
MEM_MD_DATA28 C29
MEM_MD_DATA27 E23
MEM_MD_DATA26 F24
MEM_MD_DATA25 E27
MEM_MD_DATA24 F28
MEM_MD_DATA23 F28
MEM_MD_DATA22 L31
MEM_MD_DATA21 L35
MEM_MD_DATA20 J35
MEM_MD_DATA19 M30
MEM_MD_DATA18 K30
MEM_MD_DATA17 M34
MEM_MD_DATA16 K34
MEM_MD_DATA15 E33
MEM_MD_DATA14 D32
MEM_MD_DATA13 E35
MEM_MD_DATA12 F34
MEM_MD_DATA11 E31
MEM_MD_DATA10 G31
MEM_MD_DATA9 B34
MEM_MD_DATA8 A35
MEM_MD_DATA7 K38
MEM_MD_DATA6 J38
MEM_MD_DATA5 J38
MEM_MD_DATA4 C39
MEM_MD_DATA3 M38
MEM_MD_DATA2 L37
MEM_MD_DATA1 B38
MEM_MD_DATA0 D38

DDR3_DQS_DP[17] M26
DDR3_DQS_DP[16] Y6
DDR3_DQS_DP[15] AH4
DDR3_DQS_DP[14] B8
DDR3_DQS_DP[13] M4
DDR3_DQS_DP[12] F26
DDR3_DQS_DP[11] J33
DDR3_DQS_DP[10] C38
DDR3_DQS_DP[9] L26
DDR3_DQS_DP[8] AB4
DDR3_DQS_DP[7] AK2
DDR3_DQS_DP[6] E7
DDR3_DQS_DP[5] H2
DDR3_DQS_DP[4] E25
DDR3_DQS_DP[3] M32
DDR3_DQS_DP[2] B32
DDR3_DQS_DP[1] E37
DDR3_DQS_DP[0] E37

DDR3_CKE[5] K22
DDR3_CKE[4] D22
DDR3_CKE[3] A21
DDR3_CKE[2] E21
DDR3_CKE[1] F21
DDR3_CKE[0] G15

DDR3_ODT[5] F11
DDR3_ODT[4] D12
DDR3_ODT[3] D14
DDR3_ODT[2] A13
DDR3_ODT[1] D16
DDR3_ODT[0] D16

DDR3_CS_N[9] B12
DDR3_CS_N[8] B14
DDR3_CS_N[7] CID[4]
DDR3_CS_N[6] CID[3]
DDR3_CS_N[5] CID[2]
DDR3_CS_N[4] CID[1]
DDR3_CS_N[3] CID[0]
DDR3_CS_N[2] CID[0]
DDR3_CS_N[1] CID[0]
DDR3_CS_N[0] CID[0]

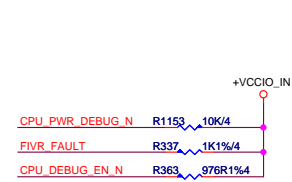
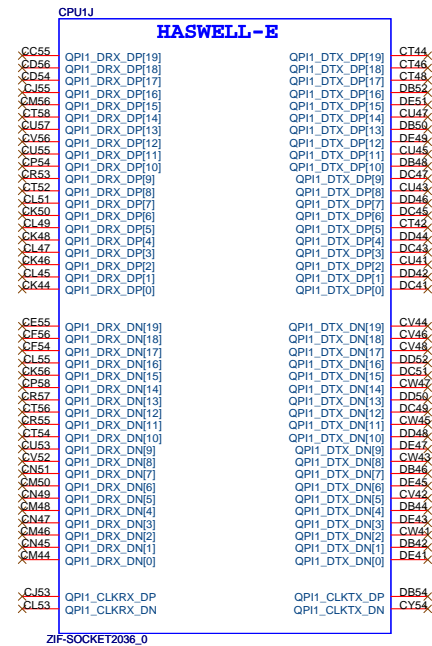
DDR3_BG[1] J11
DDR3_BG[0] J21
DDR3_ACT_N M22
DDR3_PAR J15



MICRO-STAR INT'L CO.,LTD

MS-7A21

Size	Document Description	Rev
Custom	CPU-Memory2/3	11
Date: Wednesday, July 13, 2016	Sheet 6 of 77	



VCCP	CPUIM	HASWELL-E	VCCP
BD10	VCCIN-85	VCCIN-41	BL7
BD12	VCCIN-84	VCCIN-40	BL9
BD14	VCCIN-83	VCCIN-39	BL11
BD16	VCCIN-82	VCCIN-38	BL13
BD42	VCCIN-81	VCCIN-37	BL15
BE1	VCCIN-80	VCCIN-36	BL17
BE3	VCCIN-79	VCCIN-35	BM2
BE5	VCCIN-78	VCCIN-34	BM4
BE7	VCCIN-77	VCCIN-33	BM6
BE9	VCCIN-76	VCCIN-32	BM8
BE11	VCCIN-75	VCCIN-31	BM10
BE13	VCCIN-74	VCCIN-30	BM12
BE15	VCCIN-73	VCCIN-29	BM14
BE17	VCCIN-72	VCCIN-28	BM15
BG1	VCCIN-71	VCCIN-27	BM42
BH2	VCCIN-70	VCCIN-26	BN3
BH4	VCCIN-69	VCCIN-25	BN5
BH6	VCCIN-68	VCCIN-24	BN7
BH8	VCCIN-67	VCCIN-23	BN9
BH10	VCCIN-66	VCCIN-22	BN11
BH12	VCCIN-65	VCCIN-21	BN13
BH14	VCCIN-64	VCCIN-20	BN15
BH16	VCCIN-63	VCCIN-19	BN17
BH42	VCCIN-62	VCCIN-18	BP10
BJ1	VCCIN-61	VCCIN-17	BP16
BJ3	VCCIN-60	VCCIN-16	BP42
BJ5	VCCIN-59	VCCIN-15	BR17
BJ7	VCCIN-58	VCCIN-14	BU17
BJ9	VCCIN-57	VCCIN-13	BY18
BJ11	VCCIN-56	VCCIN-12	BY20
BJ13	VCCIN-55	VCCIN-11	BY22
BJ15	VCCIN-54	VCCIN-10	BY24
BJ17	VCCIN-53	VCCIN-9	BY25
BK2	VCCIN-52	VCCIN-8	BY30
BK4	VCCIN-51	VCCIN-7	BY34
BK6	VCCIN-50	VCCIN-6	BY36
BK8	VCCIN-49	VCCIN-5	BY38
BK10	VCCIN-48	VCCIN-4	BY40
BK12	VCCIN-47	VCCIN-3	BY42
BK14	VCCIN-46	VCCIN-2	
BK16	VCCIN-45		
BL1	VCCIN-44	VCCIN_SENSE	BN1
BL3	VCCIN-43		
BL5	VCCIN-42	VSS_VCCIN_SENSE	BP2

VCCP	CPUI1	HASWELL-E	
AF42	VCCIN-173	VCCIN-129	AU11
AG23	VCCIN-172	VCCIN-128	AU13
AG27	VCCIN-170	VCCIN-127	AU15
AG29	VCCIN-172	VCCIN-126	AU17
AG33	VCCIN-169	VCCIN-125	AU2
AG35	VCCIN-168	VCCIN-124	AU4
AG39	VCCIN-167	VCCIN-123	AU6
AG41	VCCIN-166	VCCIN-122	AU8
AH42	VCCIN-165	VCCIN-121	AV10
AL17	VCCIN-164	VCCIN-120	AV12
AM42	VCCIN-163	VCCIN-119	AV14
AN11	VCCIN-162	VCCIN-118	AV16
AN17	VCCIN-161	VCCIN-117	AW1
AP22	VCCIN-160	VCCIN-116	AX42
AP4	VCCIN-159	VCCIN-115	BA1
AP6	VCCIN-158	VCCIN-114	BA3
AP8	VCCIN-157	VCCIN-113	BA5
AP10	VCCIN-156	VCCIN-112	BA7
AP12	VCCIN-155	VCCIN-111	BA9
AP14	VCCIN-154	VCCIN-110	BA11
AP16	VCCIN-153	VCCIN-109	BA13
AR1	VCCIN-152	VCCIN-108	BA15
AR3	VCCIN-151	VCCIN-107	BA17
AR5	VCCIN-150	VCCIN-106	BB2
AR7	VCCIN-149	VCCIN-105	BB4
AR9	VCCIN-148	VCCIN-104	BB6
AR11	VCCIN-147	VCCIN-103	BB8
AR13	VCCIN-146	VCCIN-102	BB10
AR15	VCCIN-145	VCCIN-101	BB12
AR17	VCCIN-144	VCCIN-100	BB14
AT2	VCCIN-143	VCCIN-99	BB16
AT4	VCCIN-142	VCCIN-98	BC1
AT6	VCCIN-141	VCCIN-97	BC3
AT8	VCCIN-140	VCCIN-96	BC5
AT10	VCCIN-139	VCCIN-95	BC7
AT12	VCCIN-138	VCCIN-94	BC9
AT14	VCCIN-137	VCCIN-93	BC11
AT16	VCCIN-136	VCCIN-92	BC13
AT42	VCCIN-135	VCCIN-91	CC15
AU1	VCCIN-134	VCCIN-90	CC17
AU3	VCCIN-133	VCCIN-89	DD2
AU5	VCCIN-132	VCCIN-88	DD4
AU7	VCCIN-131	VCCIN-87	DD6
AU9	VCCIN-130	VCCIN-86	DD8

VCCP

C268 22u6 3X/8

C267 22u6 3X/8

C308 22u6 3X/8

C269 22u6 3X/8

C222 22u6 3X/8

C239 22u6 3X/8

C237 22u6 3X/8

C107 22u6 3X/8

C996 22u6 3X/8

C232 22u6 3X/8

C1006 22u6 3X/8

C1002 22u6 3X/8

C1001 22u6 3X/8

C22 22u6 3X/8

C260 22u6 3X/8

C23 22u6 3X/8

C998 22u6 3X/8

C999 22u6 3X/8

C247 22u6 3X/8

C1003 22u6 3X/8

C246 22u6 3X/8

C249 22u6 3X/8

C264 22u6 3X/8

C223 22u6 3X/8

C233 22u6 3X/8

C1004 22u6 3X/8

C265 22u6 3X/8

C266 22u6 3X/8

PLACE 0805 CAPS INSIDE CPU SOCKET CAVITY

[illegible]

VCC_DDR_01

VCC_DDR_23

+VCCIO_IN

C985 22uF 3V6

C986 22uF 3V6

C987 22uF 3V6

C988 22uF 3V6

C989 22uF 3V6

C990 22uF 3V6

C991 22uF 3V6

C992 22uF 3V6

C101 22uF 3V6



Size Custom	Document Description CPU-Power	Rev 11
Date: Wednesday, July 13, 2016		Sheet 8 of 77

CPU-GND

CPU1N

HASWELL-E

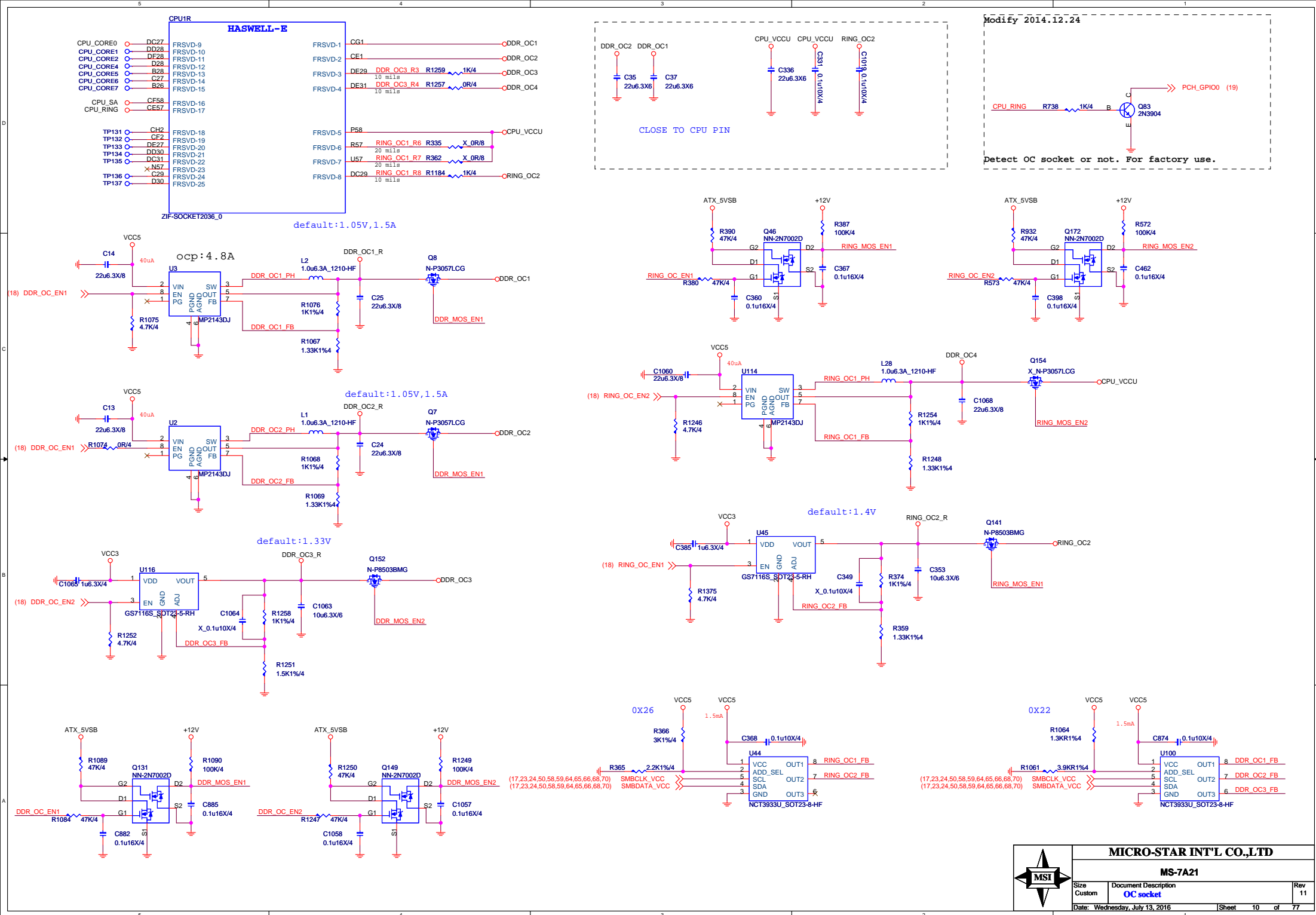
A23	VSS-629	VSS-553	M2
A37	VSS-628	VSS-551	M36
A39	VSS-627	VSS-550	M42
A41	VSS-626	VSS-549	M44
A43	VSS-625	VSS-548	M46
A45	VSS-624	VSS-547	M48
A47	VSS-623	VSS-546	M50
A49	VSS-622	VSS-545	M52
A5	VSS-631	VSS-543	N23
A51	VSS-621	VSS-542	N27
A7	VSS-619	VSS-540	N29
B10	VSS-630	VSS-541	N33
B36	VSS-618	VSS-539	N35
B40	VSS-617	VSS-538	N37
B62	VSS-616	VSS-537	N39
B6	VSS-620	VSS-536	N43
C33	VSS-615	VSS-535	N45
C5	VSS-614	VSS-534	N47
C55	VSS-613	VSS-533	N49
D10	VSS-611	VSS-532	N5
D24	VSS-610	VSS-531	N51
F50	VSS-609	VSS-530	P10
D36	VSS-608	VSS-529	P24
D40	VSS-607	VSS-528	P26
E1	VSS-606	VSS-527	P28
E3	VSS-605	VSS-526	P30
E39	VSS-604	VSS-525	P32
F41	VSS-603	VSS-524	P34
F2	VSS-602	VSS-523	P36
F30	VSS-601	VSS-522	P40
F32	VSS-599	VSS-521	P54
F36	VSS-598	VSS-520	P56
F4	VSS-597	VSS-519	R11
F42	VSS-596	VSS-518	R25
F44	VSS-595	VSS-517	R29
F48	VSS-594	VSS-516	R31
F50	VSS-593	VSS-515	R33
G1	VSS-592	VSS-514	R35
G23	VSS-591	VSS-513	R37
G27	VSS-590	VSS-512	R39
G33	VSS-589	VSS-511	R41
G35	VSS-588	VSS-510	R43
G39	VSS-587	VSS-509	R45
G41	VSS-586	VSS-508	R47
G45	VSS-585	VSS-507	R49
G47	VSS-584	VSS-506	R51
G49	VSS-583	VSS-505	R53
G5	VSS-582	VSS-504	R55
G51	VSS-581	VSS-503	R57
G57	VSS-580	VSS-502	R59
G9	VSS-579	VSS-501	R61
H24	VSS-577	VSS-500	R63
H26	VSS-576	VSS-499	R65
H28	VSS-575	VSS-498	R67
H30	VSS-574	VSS-497	R69
H32	VSS-573	VSS-496	R71
H34	VSS-572	VSS-495	R73
H36	VSS-571	VSS-494	R75
H40	VSS-570	VSS-493	R77
H54	VSS-569	VSS-492	R79
H6	VSS-579	VSS-491	R81
H8	VSS-578	VSS-490	R83
J25	VSS-567	VSS-489	R85
J29	VSS-566	VSS-488	R87
J3	VSS-565	VSS-487	R89
J31	VSS-564	VSS-486	R91
J37	VSS-563	VSS-485	R93
J5	VSS-562	VSS-484	R95
J55	VSS-561	VSS-483	R97
J7	VSS-560	VSS-482	R99
K10	VSS-559	VSS-481	R101
K36	VSS-558	VSS-480	R103
K40	VSS-557	VSS-479	R105
L29	VSS-556	VSS-478	R107
L39	VSS-555	VSS-477	R109
L41	VSS-554	VSS-476	R111
L5	VSS-553	VSS-475	R113
M10	VSS-552	VSS-474	R115

ZIF-SOCKET2036_0

CPU1O

HASWELL-E

Y36	VSS-472	VSS-394	AH6
Y42	VSS-480	VSS-393	AH14
Y46	VSS-471	VSS-392	AH58
Y56	VSS-470	VSS-391	AJ11
AA3	VSS-469	VSS-390	AJ17
AA25	VSS-467	VSS-389	AK4
AA29	VSS-466	VSS-388	AK6
AA7	VSS-468	VSS-387	AK16
AA31	VSS-465	VSS-386	AK42
AA39	VSS-464	VSS-385	AK44
AA55	VSS-463	VSS-384	AK46
AB12	VSS-462	VSS-383	AK48
AB36	VSS-461	VSS-382	AK50
AB40	VSS-460	VSS-381	AK52
AB42	VSS-459	VSS-380	AL11
AC7	VSS-458	VSS-379	AL43
AC9	VSS-457	VSS-378	AL45
AC11	VSS-456	VSS-377	AL47
AC29	VSS-455	VSS-376	AL49
AD4	VSS-454	VSS-375	AL51
AD8	VSS-452	VSS-374	AL53
AD6	VSS-453	VSS-373	AM2
AD10	VSS-451	VSS-372	AM4
AD12	VSS-450	VSS-371	AM6
AD36	VSS-449	VSS-370	AM8
AD40	VSS-448	VSS-369	AM10
AD42	VSS-447	VSS-368	AM12
AD44	VSS-446	VSS-367	AM14
AD46	VSS-445	VSS-366	AM16
AD48	VSS-444	VSS-365	AM56
AD50	VSS-443	VSS-364	AN1
AD52	VSS-442	VSS-363	AN3
AE13	VSS-441	VSS-362	AN5
AE15	VSS-440	VSS-361	AN7
AE19	VSS-439	VSS-360	AN9
AE23	VSS-438	VSS-359	AN13
AE27	VSS-437	VSS-358	AN15
AE29	VSS-436	VSS-357	AN55
AE33	VSS-435	VSS-356	AN57
AE35	VSS-434	VSS-355	AP42
AE39	VSS-433	VSS-354	AP44
AE41	VSS-432	VSS-353	AP58
AE43	VSS-431	VSS-352	AT44
AE47	VSS-430	VSS-351	AT46
AE49	VSS-429	VSS-350	AT48
AE10	VSS-428	VSS-349	AT50
AE16	VSS-427	VSS-348	AT52
AF18	VSS-426	VSS-347	AU45
AF21	VSS-425	VSS-346	AU47
AF51	VSS-424	VSS-345	AU49
AF53	VSS-423	VSS-344	AU51
AF4	VSS-422	VSS-343	AU53
AF6	VSS-421	VSS-342	AV42
AF8	VSS-420	VSS-341	AV54
AF20	VSS-419	VSS-340	AV56
AF22	VSS-418	VSS-339	AW11
AF24	VSS-417	VSS-338	AW13
AF26	VSS-416	VSS-337	AW15
AF28	VSS-415	VSS-336	AW17
AF30	VSS-414	VSS-335	AW3
AF32	VSS-413	VSS-334	AW5
AF34	VSS-412	VSS-333	AW7
AF36	VSS-411	VSS-332	AW9
AF38	VSS-410	VSS-331	AW55
AF40	VSS-409	VSS-330	AW57
AF54	VSS-408	VSS-329	AY2
AF56	VSS-407	VSS-328	AY4
AG11	VSS-406	VSS-327	AY6
AG17	VSS-405	VSS-326	AY8
AG19	VSS-404	VSS-325	AY10
AG21	VSS-403	VSS-324	AY12
AG25	VSS-402	VSS-323	AY14
AG29	VSS-401	VSS-322	AY16
AG31	VSS-400	VSS-321	AY44
AG37	VSS-399	VSS-320	BB42
AG43	VSS-398	VSS-319	BB46
AG55	VSS-397	VSS-318	BB50
AG57	VSS-396	VSS-317	BB58
AH2	VSS-395	VSS-316	BC45



DIMM1A

**MS-7A21**Document Description
DDR IV DIMM

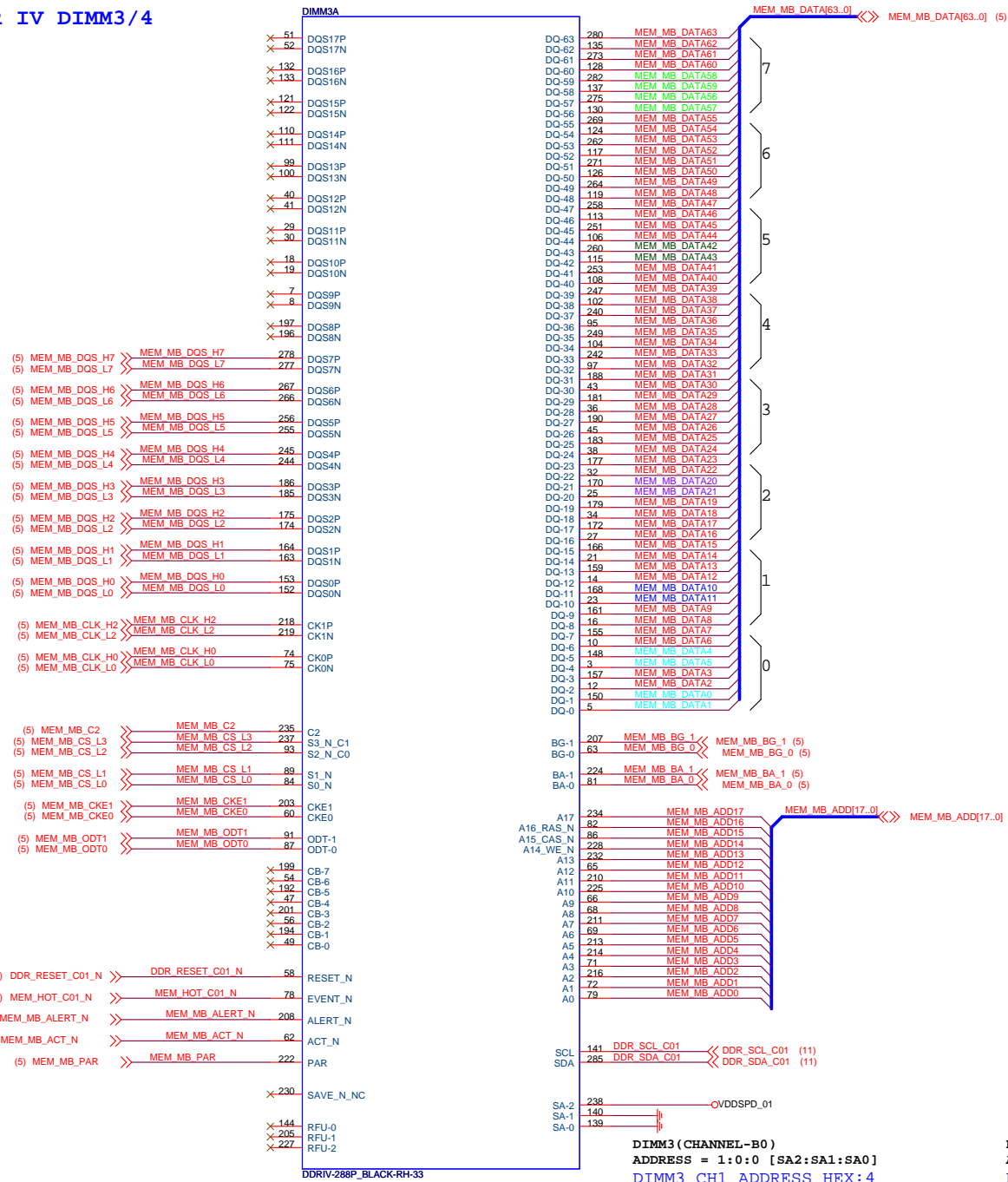
Date: Wednesday, Jul 19, 2012

Rev
11

Sheet 11 of 77

DDR IV DIMM3/4

DIMM3A



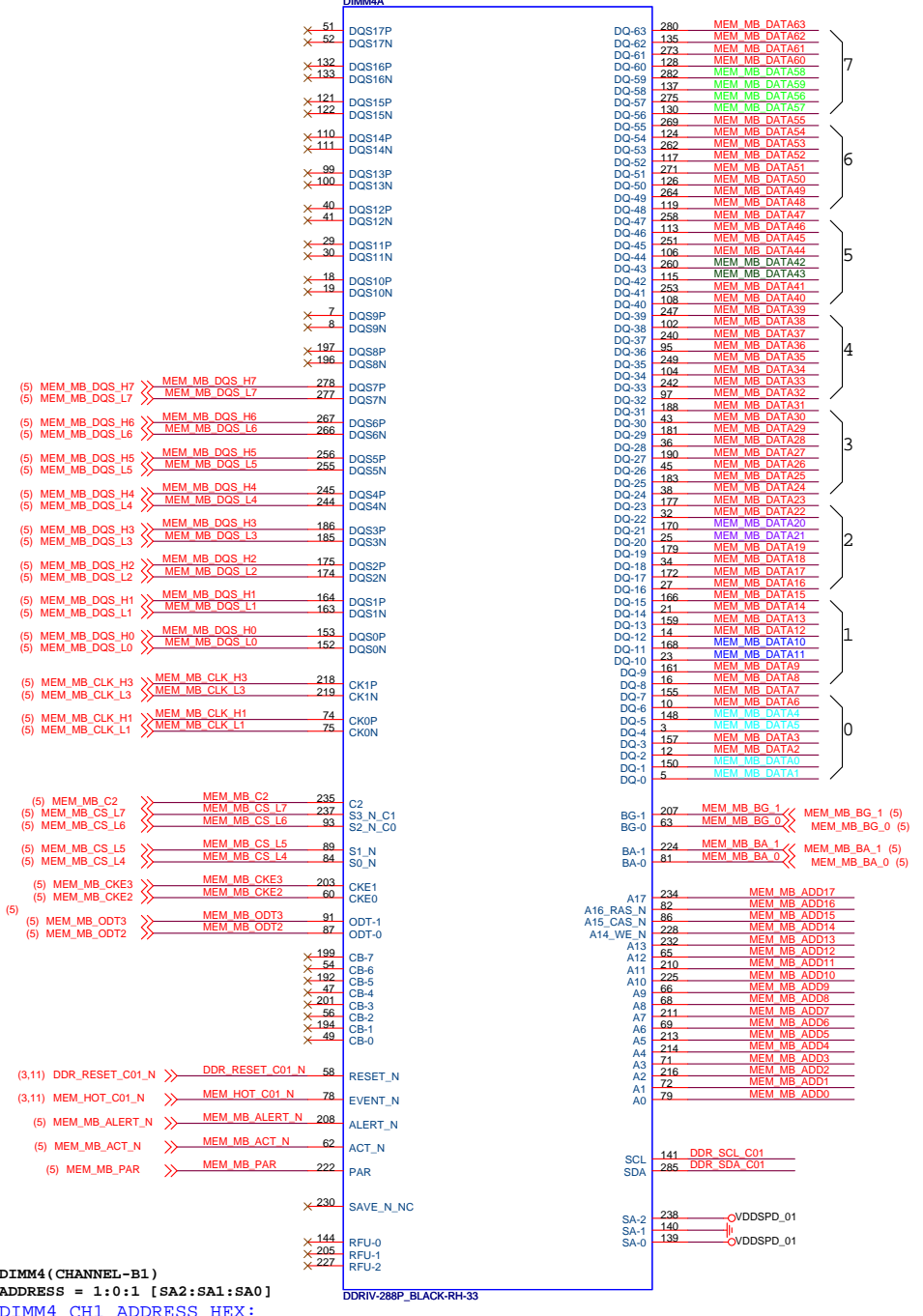
DIMM3 (CHANNEL-B0)

ADDRESS = 1:0:0 [SA2:SA1:SA0]

DIMM3 CH1 ADDRESS HEX:4

MEM_MB_DATA[63..0] (5)

DIMM4A



DIMM4 (CHANNEL-B1)

ADDRESS = 1:0:1 [SA2:SA1:SA0]

DIMM4 CH1 ADDRESS HEX:

DDRIV-288P_BLACK-RH-33

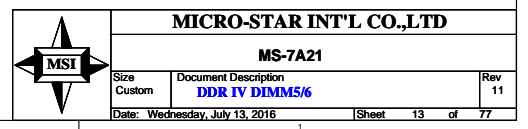
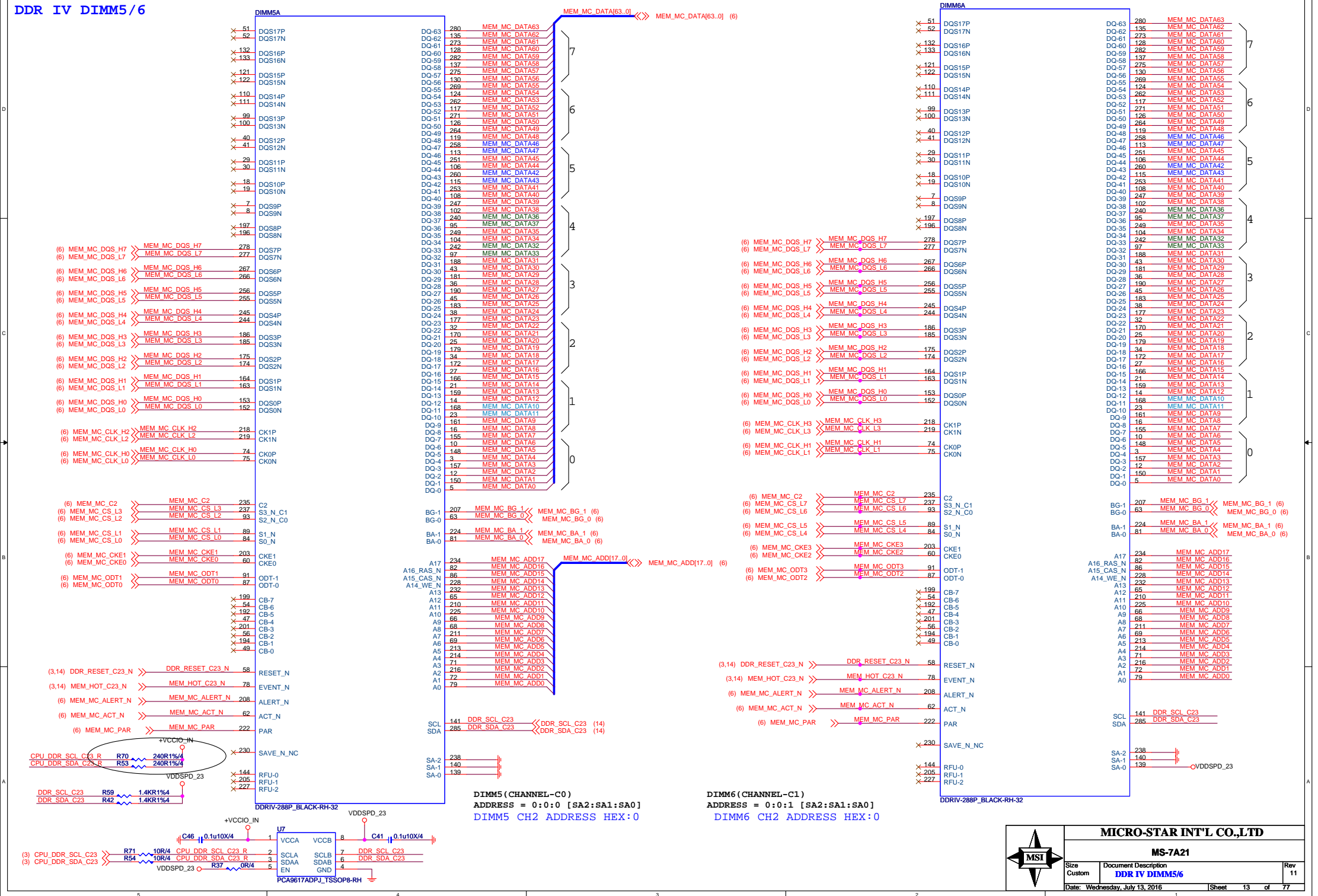


MICRO-STAR INT'L CO.,LTD

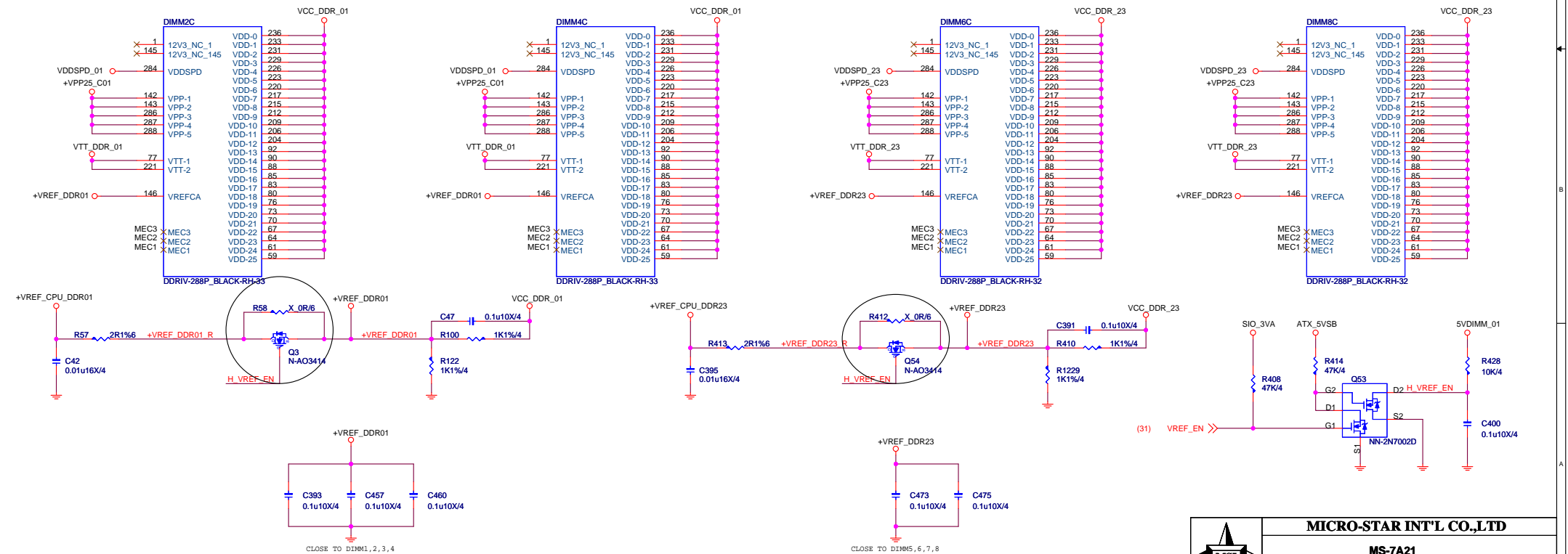
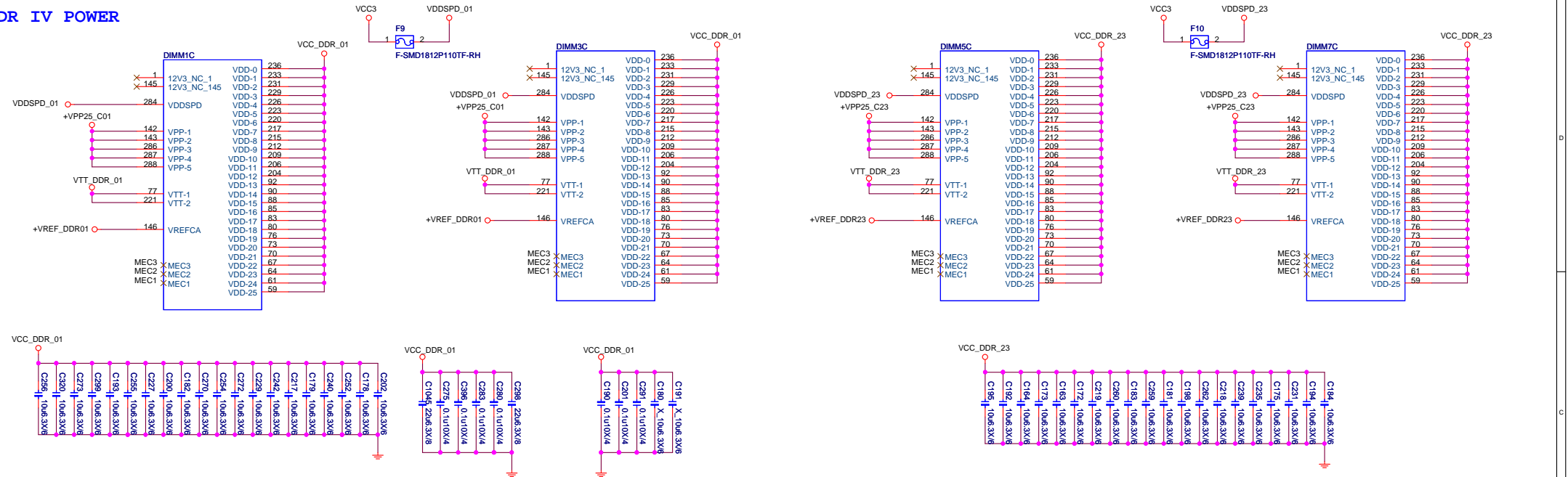
MS-7A21

Size	Document Description	Rev
Custom	DDR IV DIMM3/4	11
Date: Wednesday, July 13, 2016	Sheet 12 of 77	

DDR IV DIMM5/6



DDR IV POWER



MICRO-STAR INT'L CO.,LTD

MS-7A21

Size Custom	Document Description DDR IV POWER	Rev 11
Date: Wednesday, July 13, 2016		Sheet 15 of 77

DIMM1B

2	VSS-93	VSS-46
---	--------	--------

2 VSS-93 VSS-46

2 VSS-93 VSS-4

VSS 02	VSS 46
--------	--------

VSS 02	VSS 46
--------	--------

VSS 03	VSS 16
--------	--------

VSS-93	VSS-46
VSS-92	VSS-45

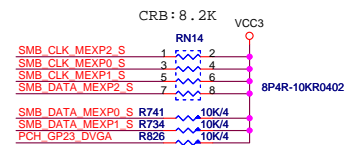
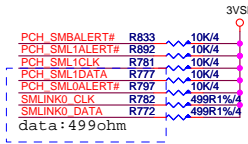


description

Custom **DDR IV GND**

Date: Wednesday, July 13, 2016 Sheet 16 of 1

PCH-LPC/HDA/RTC/MISC/SPI



SMB DATA MEXP1 S R735 X 10K/4
LT DEBUG MODE ENABLE

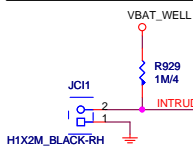
HIGH: NORMAL MODE (DEFAULT)
LOW : LT DEBUG MODE

SMB_DATA_MEXP0_S R740 X_10K/4

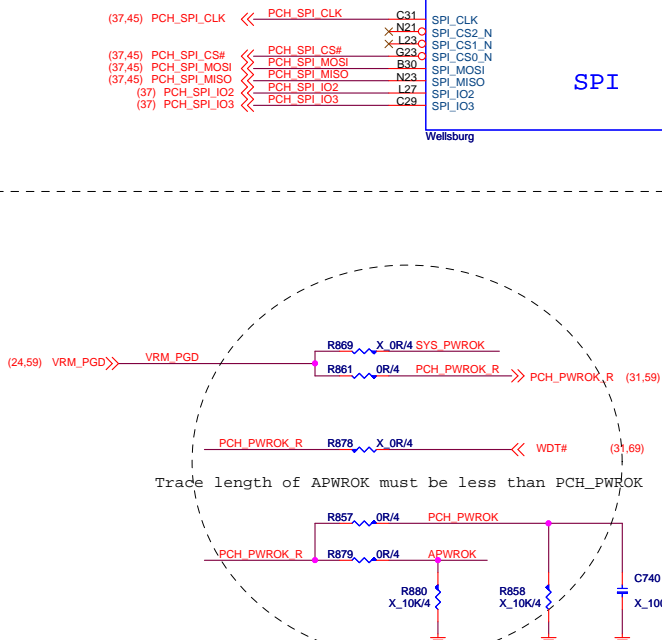
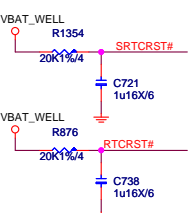
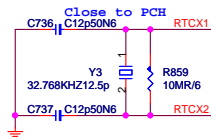
ADR TIMER HOLD OFF (DEFENSIVE)

NOTE: IAT PG ON SME
HIGH: NORMAL MODE (DEFAULT)
LOW : ADR TIMER HOLD OFF

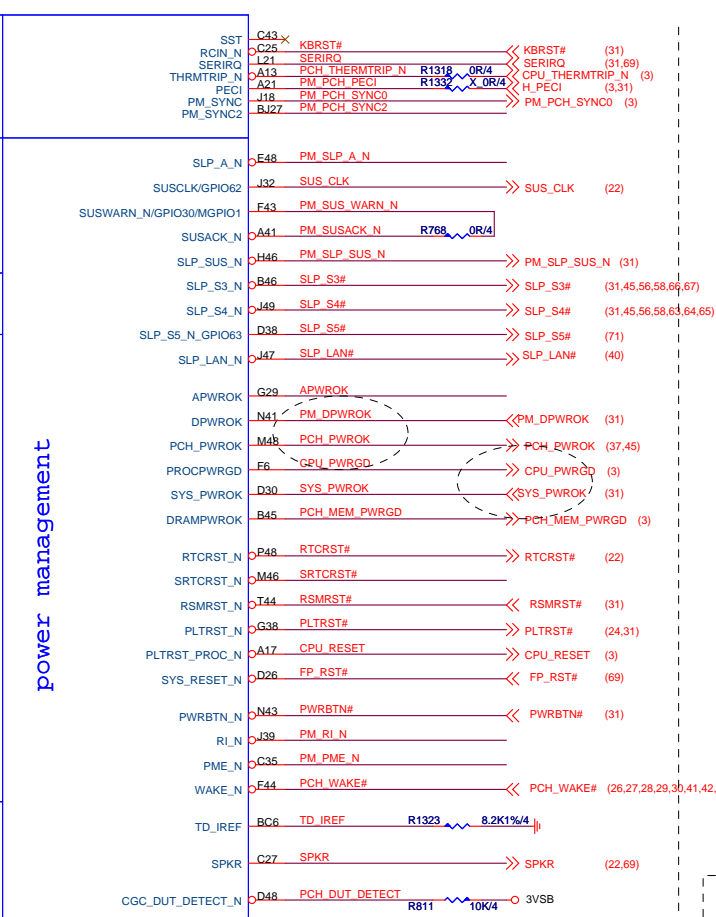
Chassis Intrusion



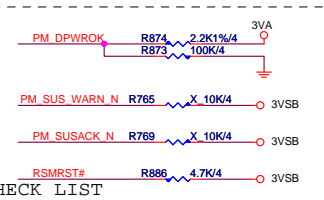
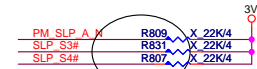
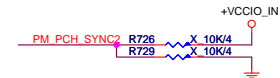
RTC Block



Trade length of APWROK must be less than PCH_PWROK



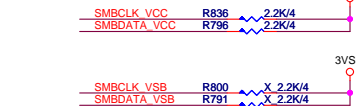
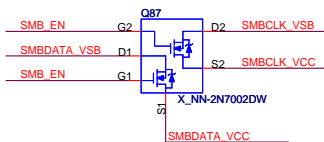
The negative min timing implies that DRAMPWROK must either fall before SLP_S4# or within 100 ns after it.



CHECK LIST



CHECK LIST



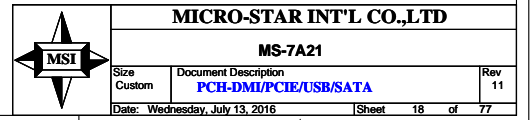
MICRO-STAR INT'L CO.,LTD

MS-7A21

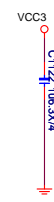
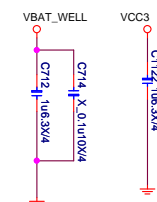
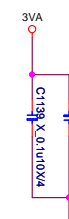
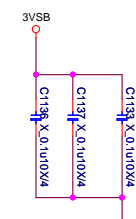
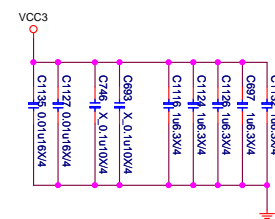
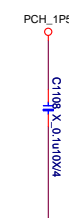
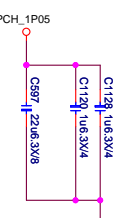
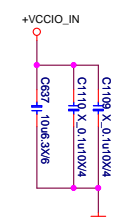
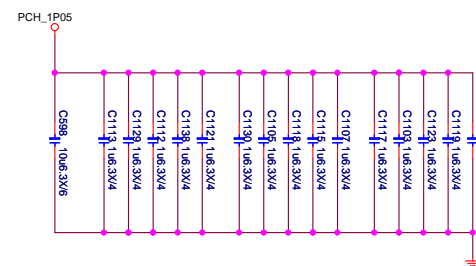
Size Custom	Document Description PCH-LPC/HDA/RTC/MISC/SPI
----------------	---------------------------------------------------------

Rev	11
-----	----

PCH1B

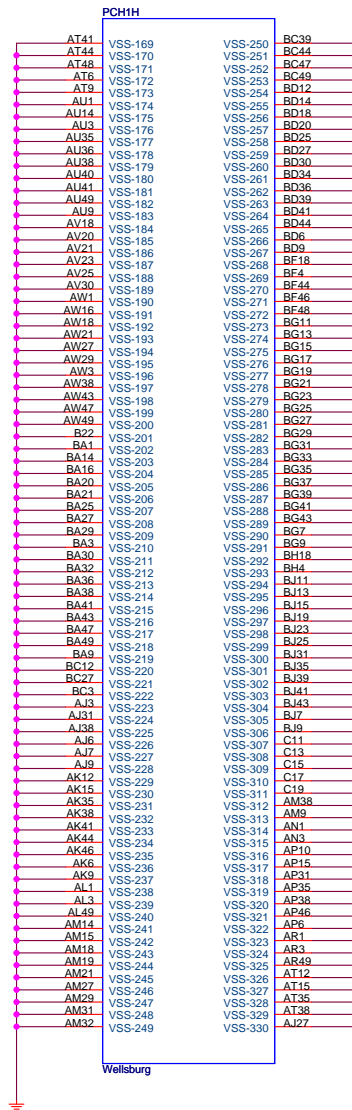
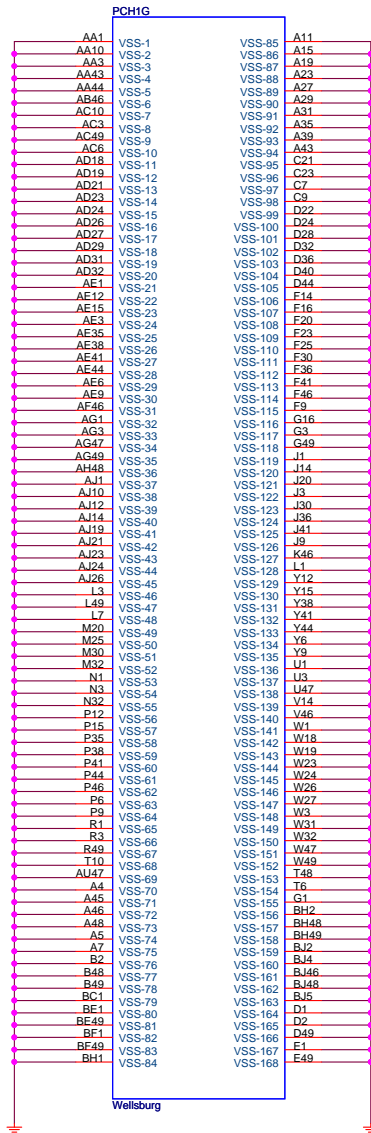


+VCCIO IN:0.004A



Rev	11
-----	----

Date: Wednesday, July 13, 2016 Sheet 20 of 77

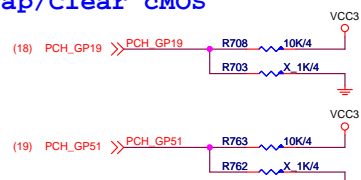


MICRO-STAR INT'L CO.,LTD

MS-7A21

Size	Document Description	Rev
Custom	PCH-GND	11
Date: Wednesday, July 13, 2016		Sheet 21 of 77

PCH Strap/Clear CMOS



	GP19	GP51
SPI	1	1
LPC	0	0

DMI RX Termination

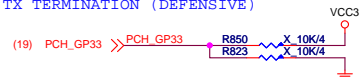


This signal has a weak internal pull-down.
This signal only take effect if DMI is configured in AC-coupled mode.
0 = DMI RX is terminated to VSS.
1 = option not supported.

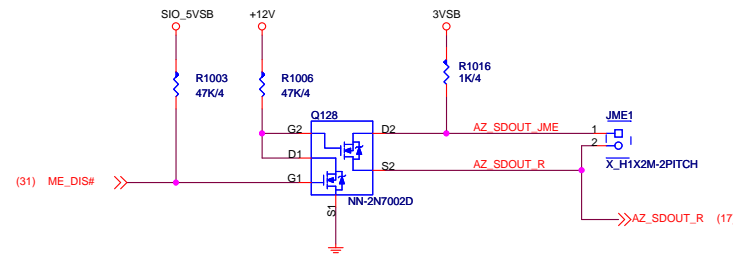


TLS CONFIDENTIALITY ENABLE STRAP
HIGH :TLS CONFIDENTIALITY ENABLE (DEFAULT)
LOW : RING OSCILLATOR BYPASS
LOW :TLS CONFIDENTIALITY DISABLE

DMI TX TERMINATION (DEFENSIVE)



This signal has a weak internal pull-down.
This signal only takes effect if DMI is configured in DC-coupled mode.
0 = DMI TX is terminated to VSS.
1 = DMI TX is terminated to VCC/2.



HIGH (1-2):SECURITY MEASURES OVERRIDEN
LOW (0-1) : SECURITY PER FLASH DESCRIPTOR (DEFAULT)

DEEP SLEEP WELL ON-DIE VRM ENABLE



HIGH: ENABLE (INTERNAL SUPPLY) (DEFAULT)
LOW: DISABLE (EXTERNAL SUPPLY)

NO REBOOT OPTION STRAP
LOW : REBOOT
HIGH: NO-REBOOT



INTEGRATED SUS 1.05V VRM ENABLE



HIGH: ENABLE (INTERNAL SUPPLY) (DEFAULT)
LOW: DISABLE (EXTERNAL SUPPLY)

PLL ON-DIE VR ENABLE



HIGH :PLL ON-DIE VR ENABLE. INT PU. (DEFAULT)
LOW :PLL ON-DIE VR DISABLE

Top-Block Swap Override



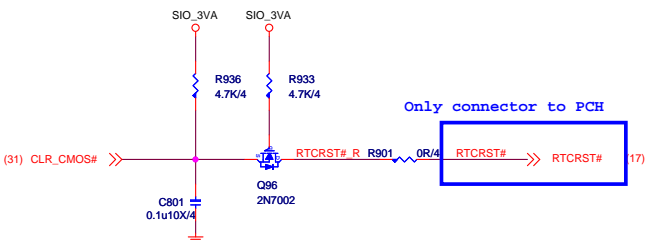
DMI AC Coupling

CHECK LIST

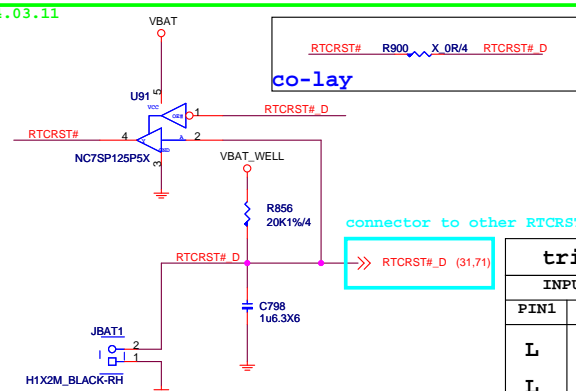


This Signal has a weak internal pull-up.
0= Configures DMI for AC coupling mode.
1 = Configures DMI for DC coupling mode.

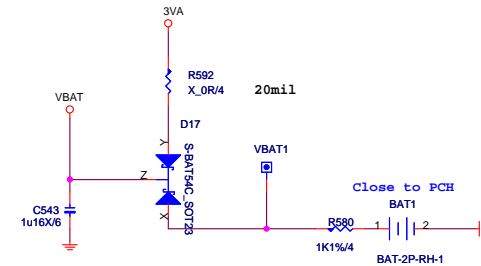
RTC and CLR_CMOS



2014.03.11



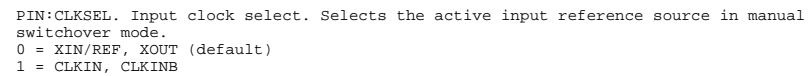
tri-state		
INPUT		outout pin4
PIN1	PIN2	
L	H	H
L	L	L
H	X	Z

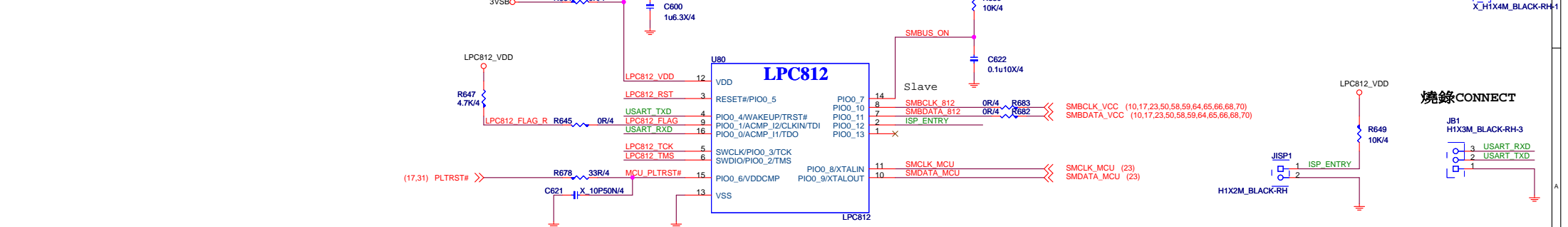
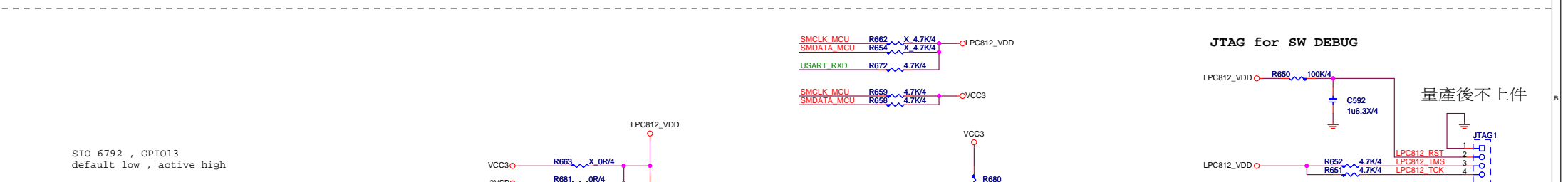
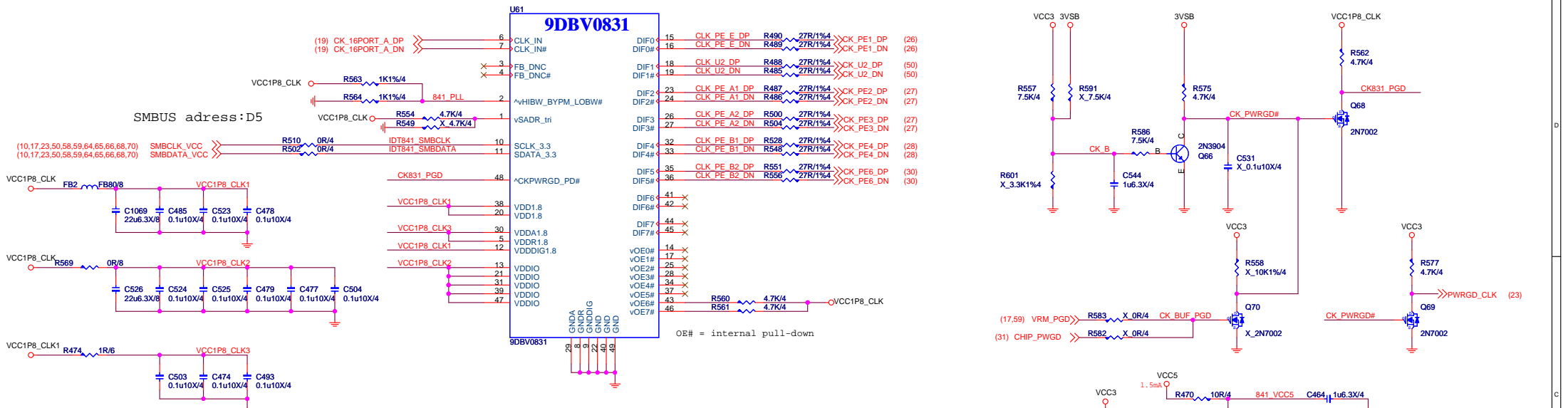


MICRO-STAR INT'L CO.,LTD

MS-7A21

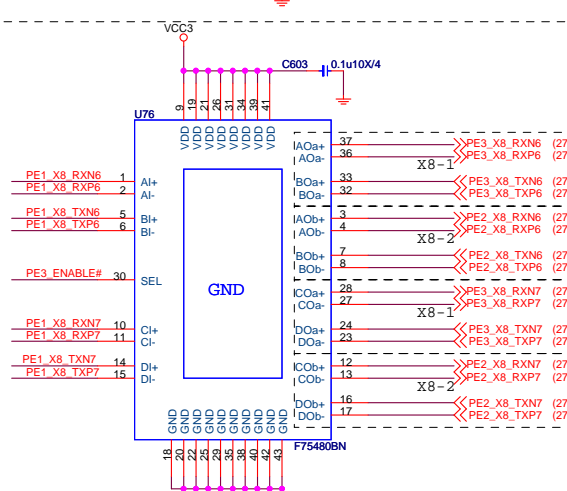
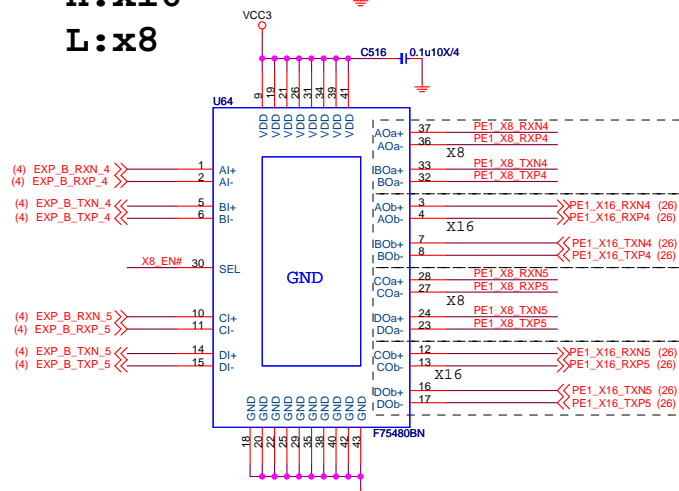
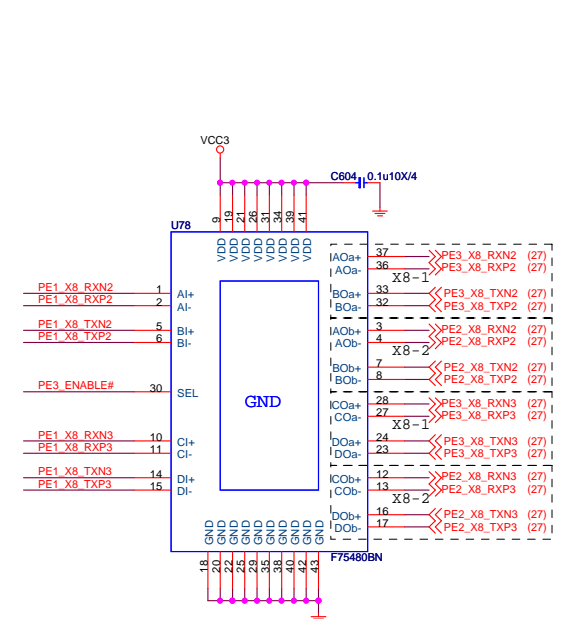
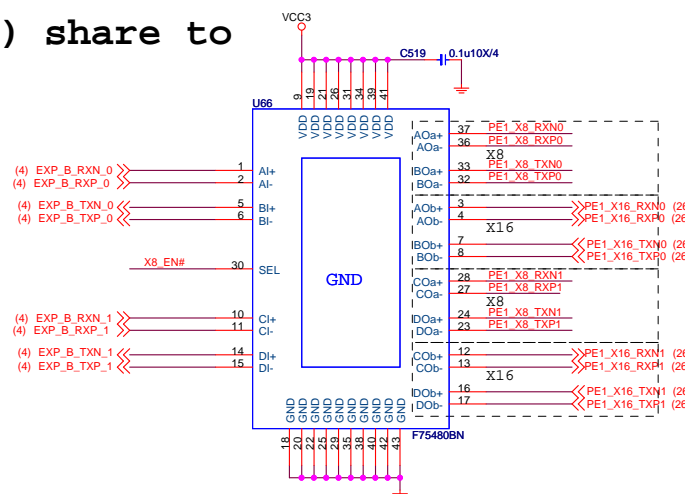
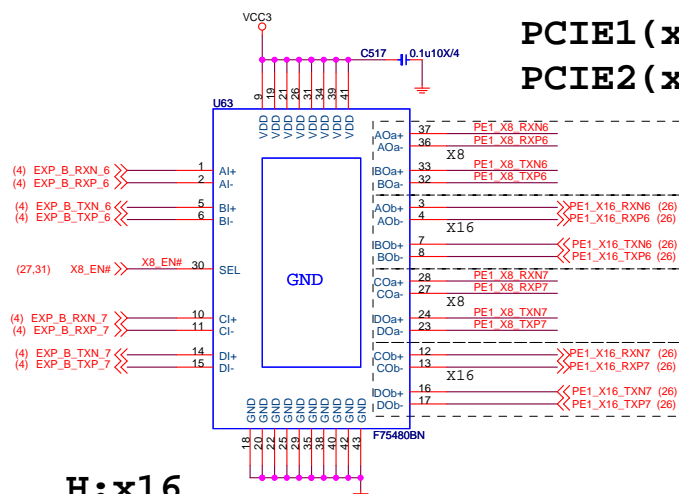
Size	Document Description	Rev
Custom	PCH Strap/Clear CMOS	11
Date:	Wednesday, July 13, 2016	Sheet 22 of 77



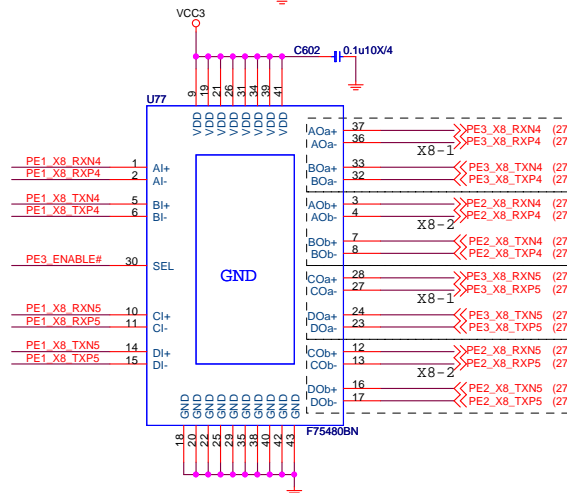
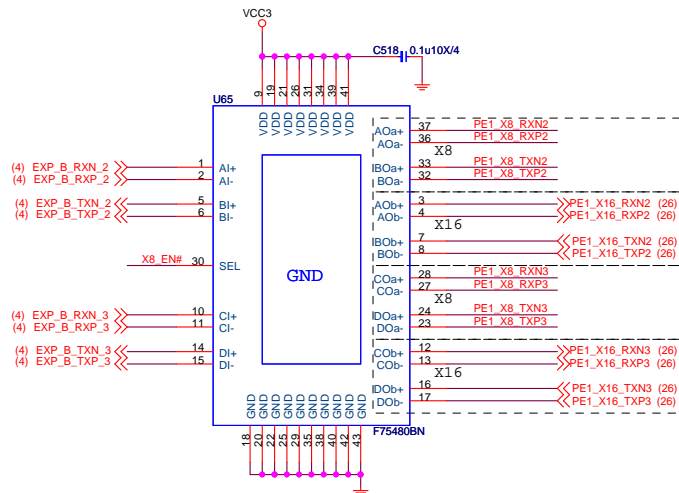
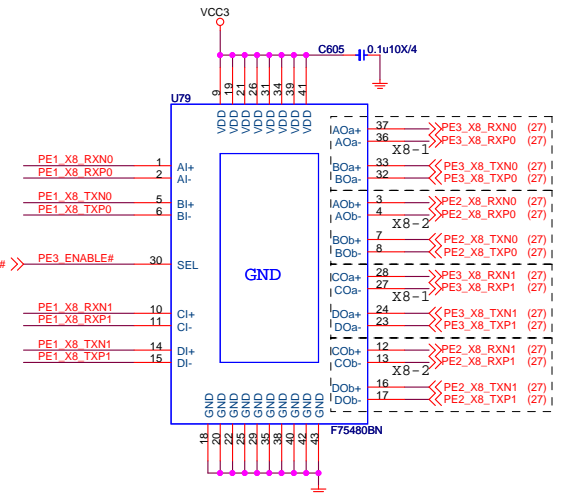


MSI			MICRO-STAR INT'L CO.,LTD		
MS-7A21			Rev 11		
Size	Document Description	Date: Wednesday, July 13, 2016	Sheet	24	of 77
Custom	CLK BUFFER831/MCU812				

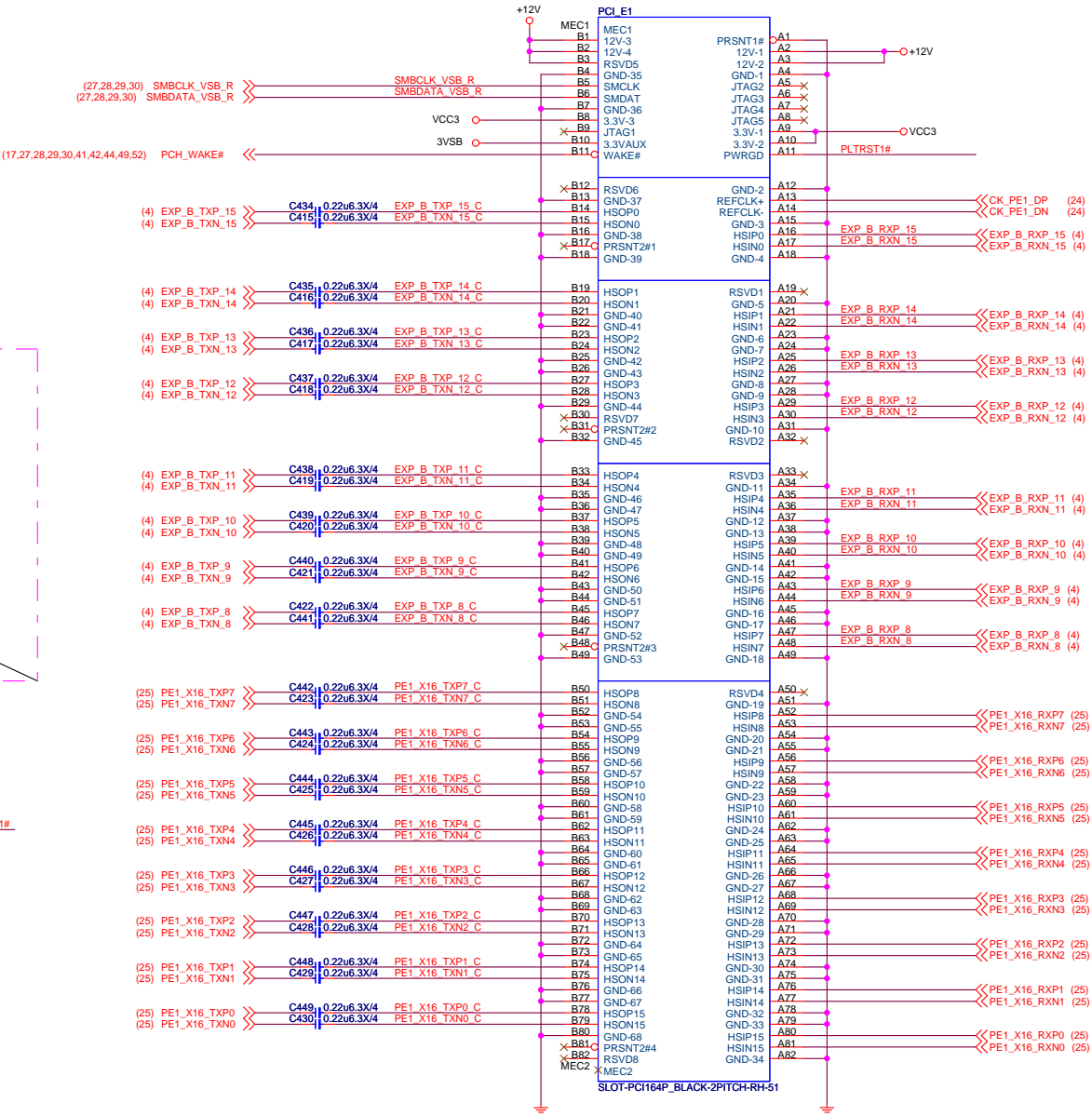
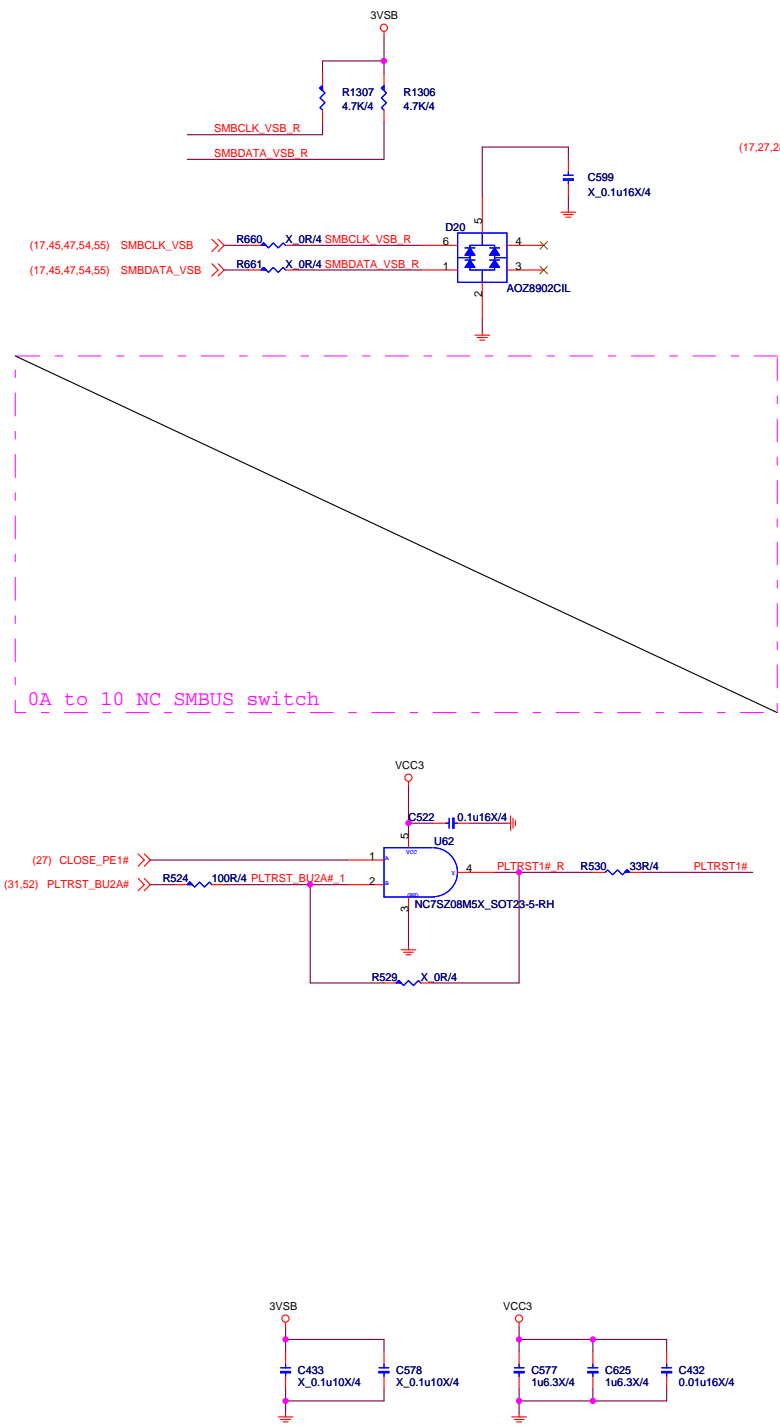
PCIE1(x16) share to PCIE2(x8)

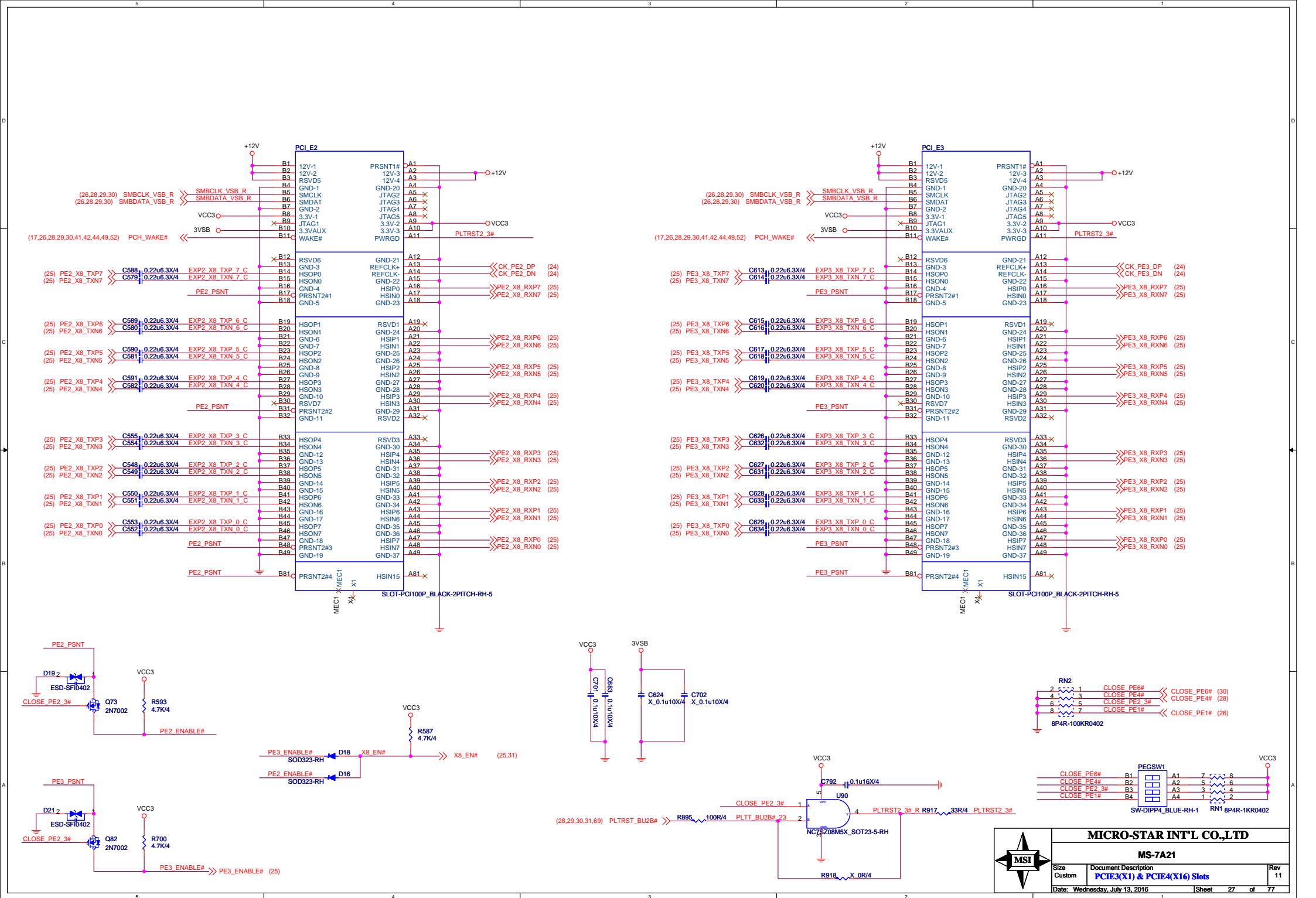


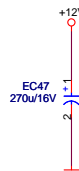
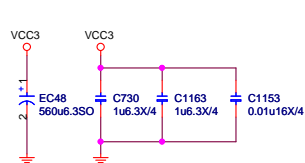
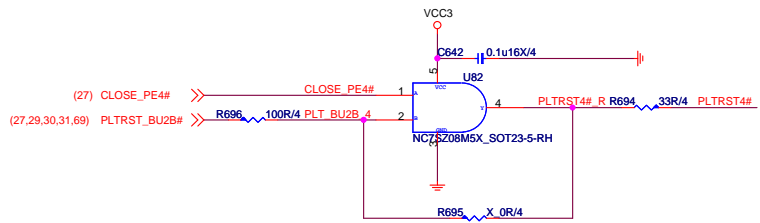
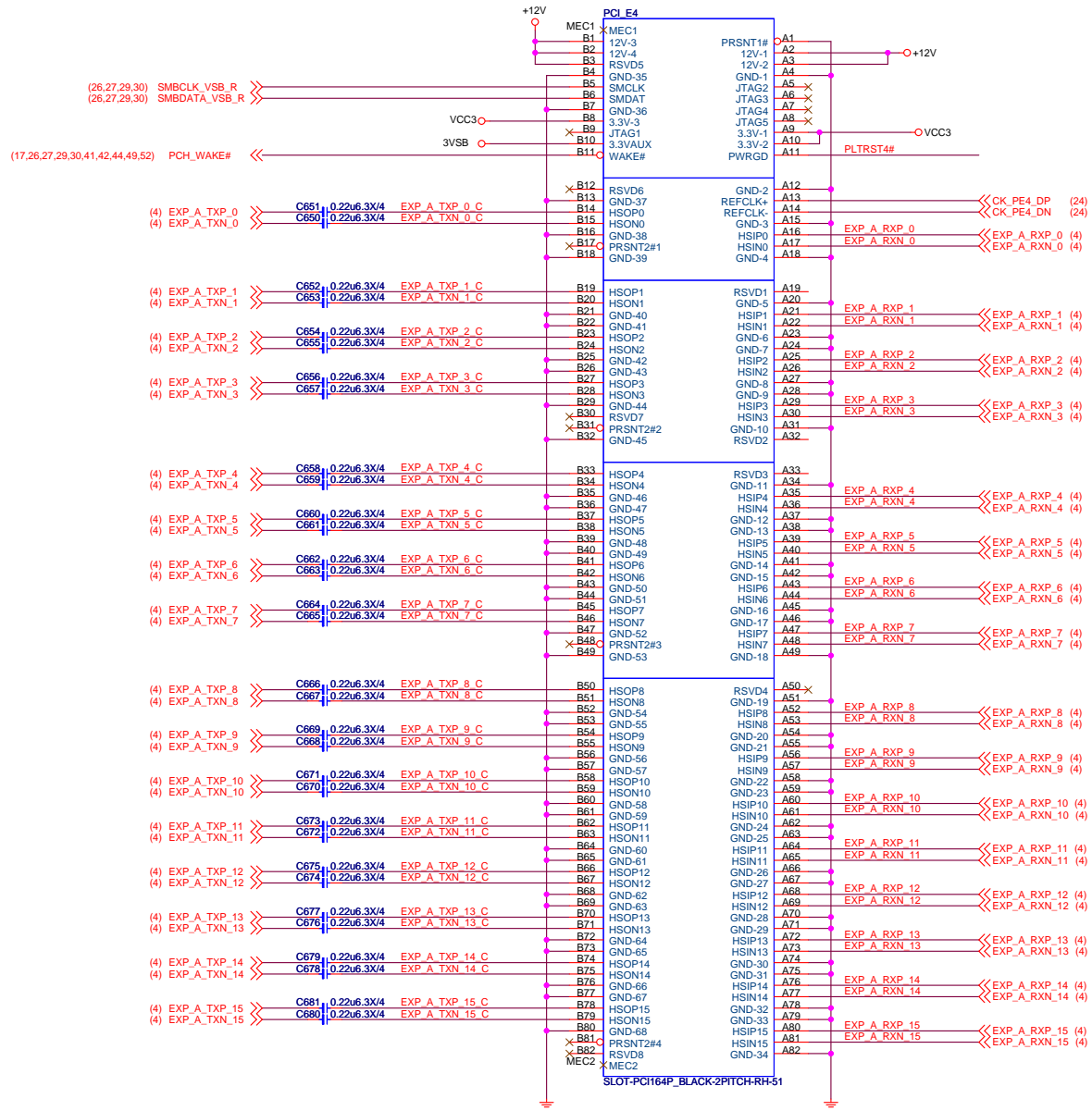
H:x8-E2
L:x8-E3

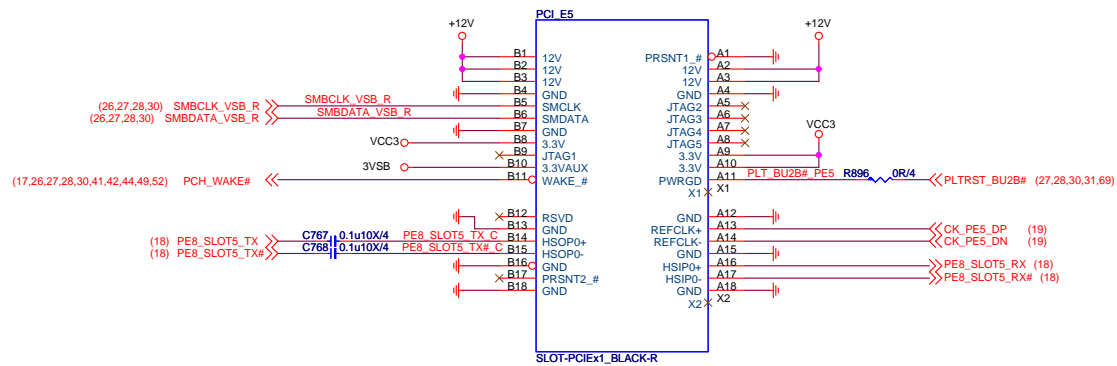


PCIE1(X16) & PCIE2(X1) Slots

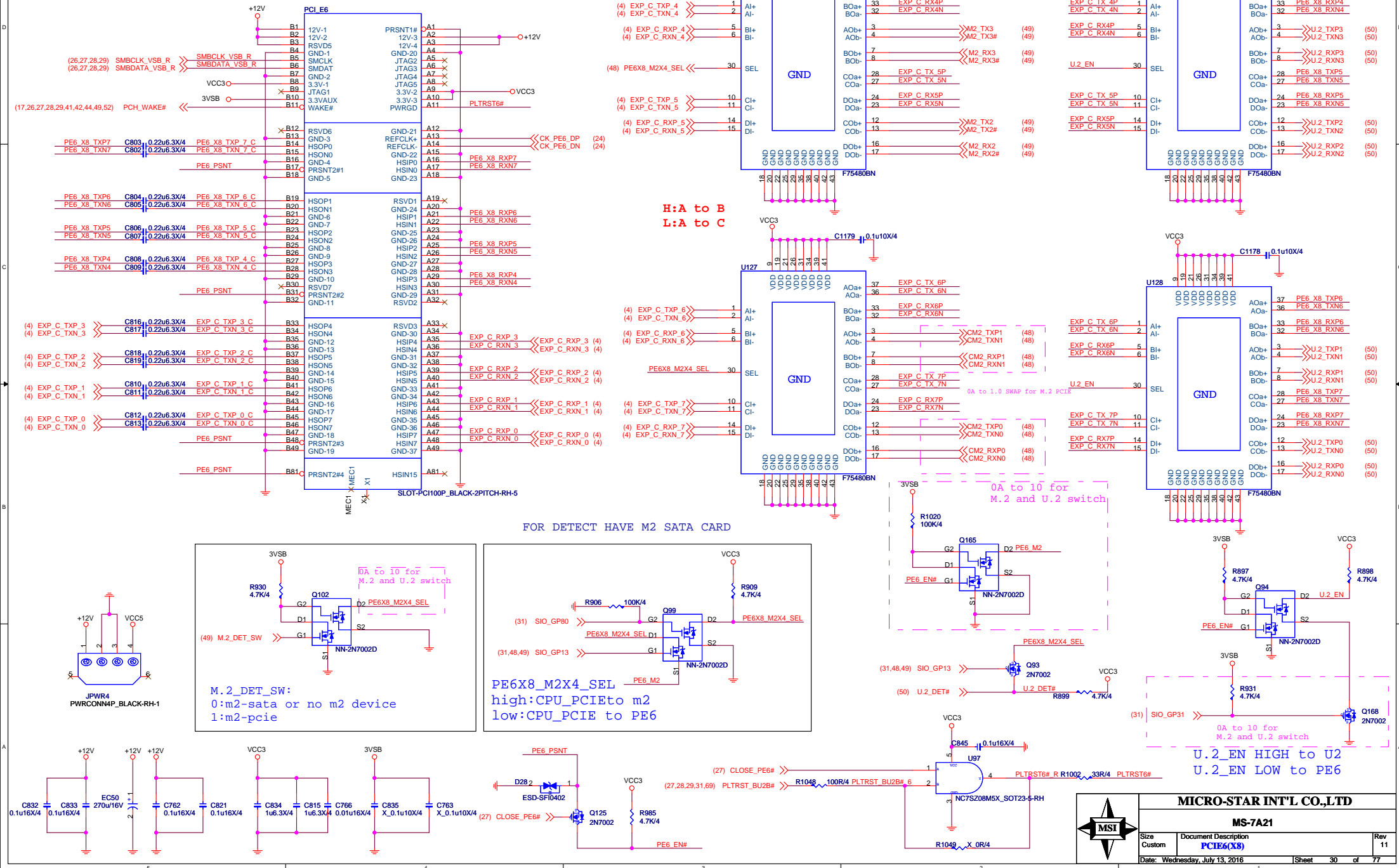




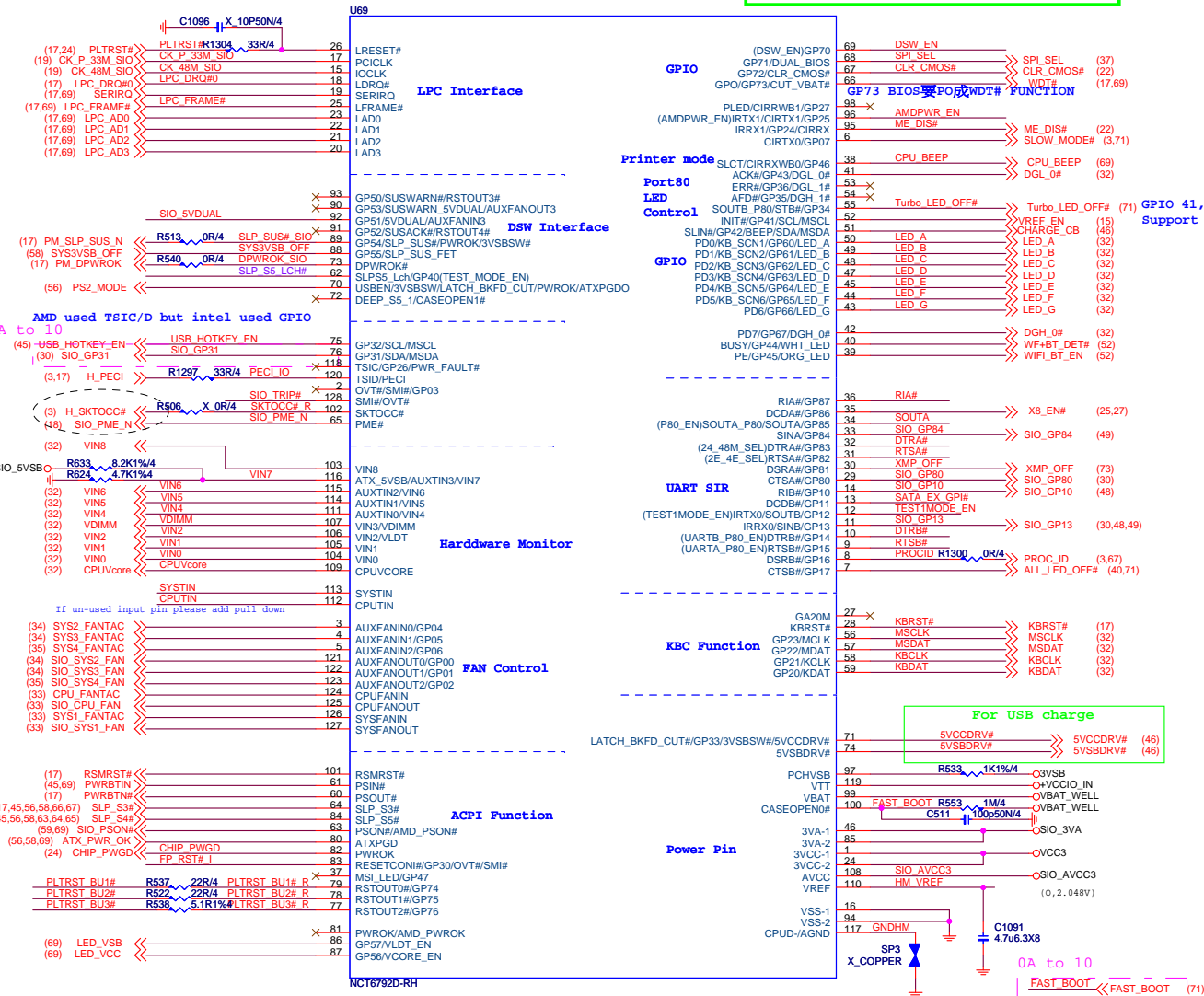




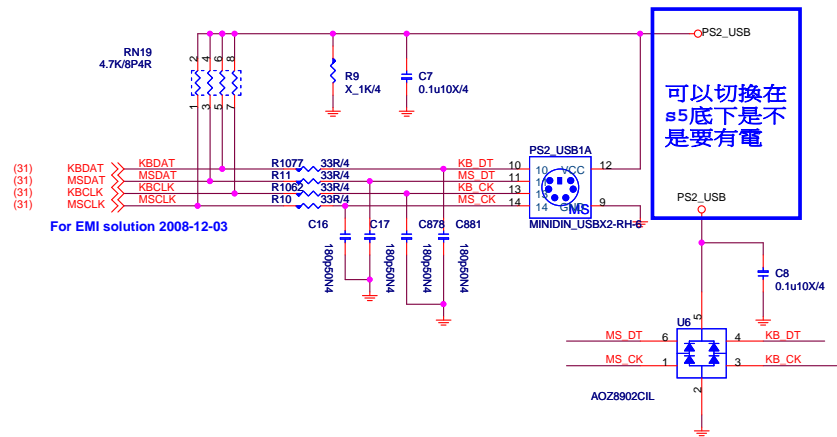
PCIe6 (x8)



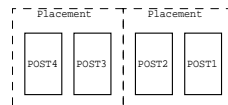
SIO-NTC6792D/PS2



PS2 KEYBOARD & MOUSE CONNECTOR

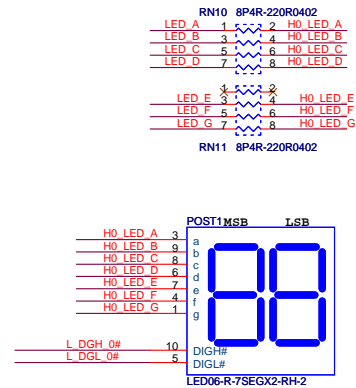
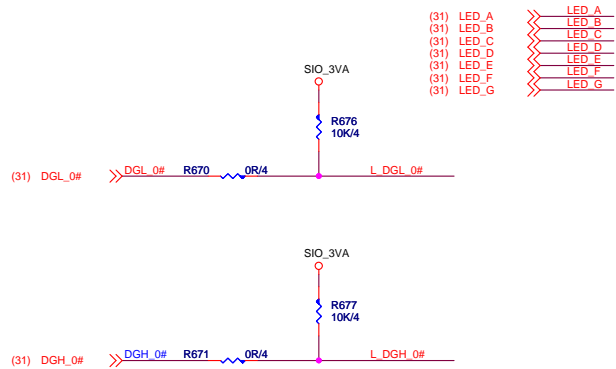


DEBUG LED

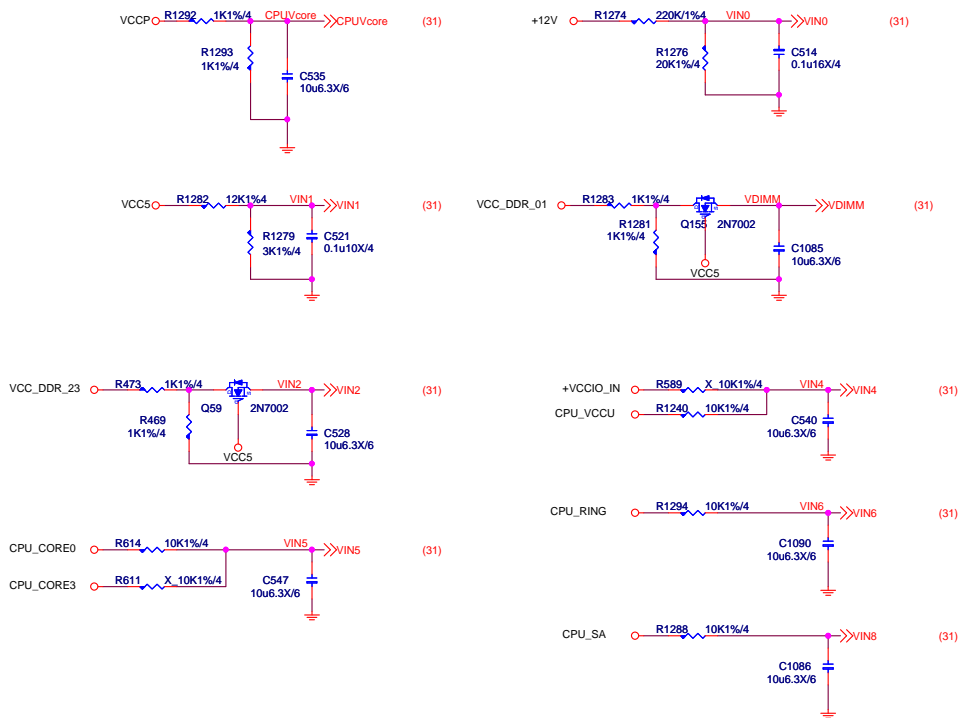


Placement一定要對

(DGH1=Post4/DGL1=Post3/DGH0=Post2/DGL0=Post1)



HW Monitor - Voltage



MSI_LED

0A to 10 remove



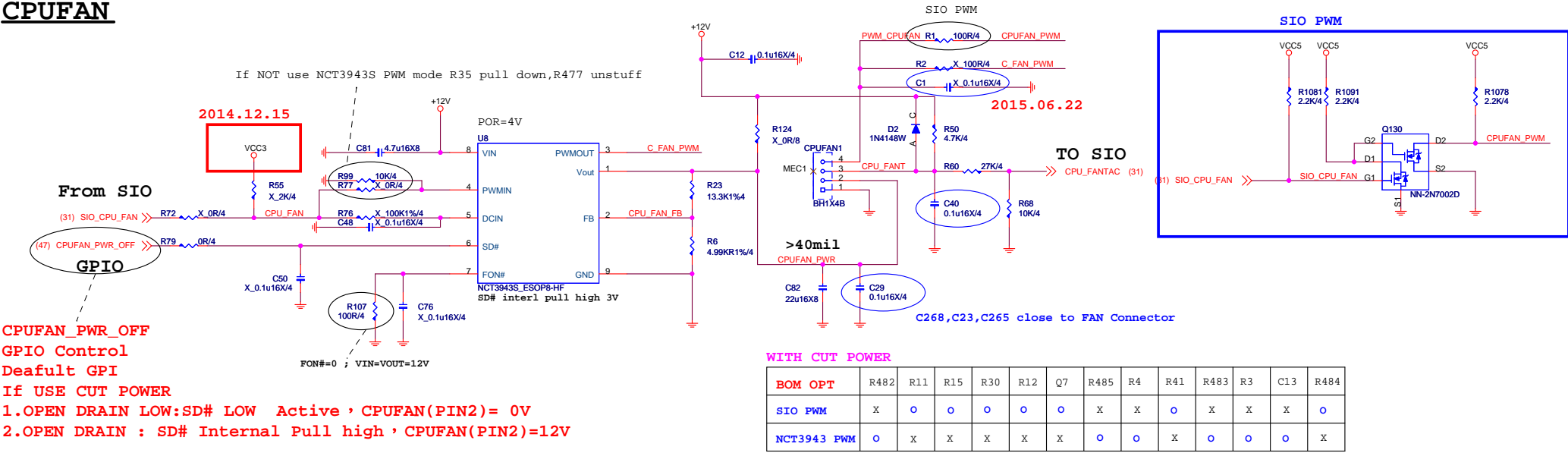
MICRO-STAR INT'L CO.,LTD

MS-7A21

Size Custom	Document Description SIO-NTC6792D/PS2	Rev 11
Date: Wednesday, July 13, 2016		Sheet 32 of 77

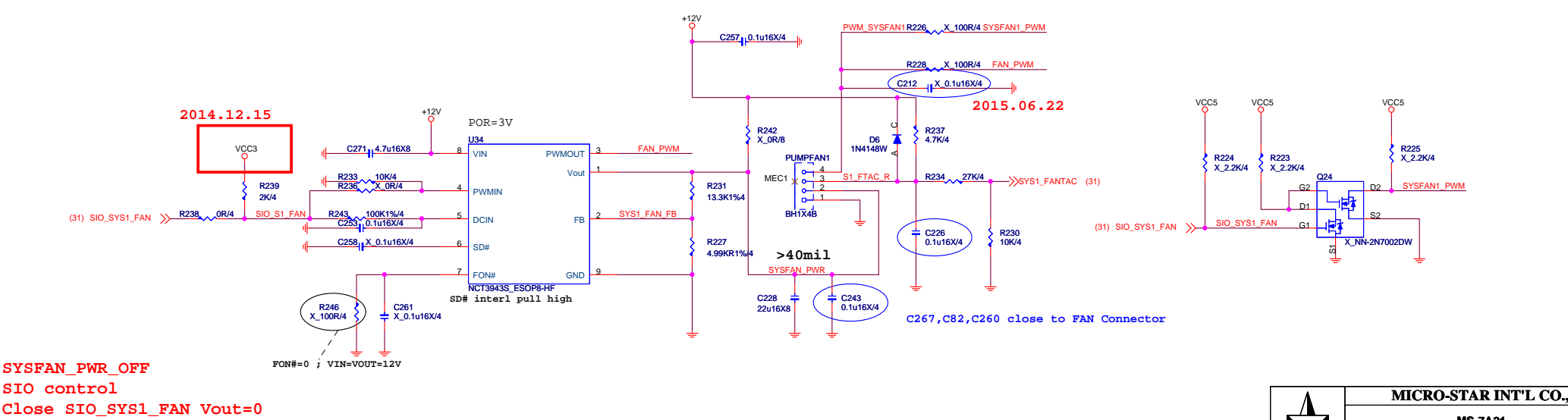
Type I : 4 PIN CPU FAN USE SIO PWM (STUFF NCT3943S WITH GPIO CUT POWER)

CPUFAN



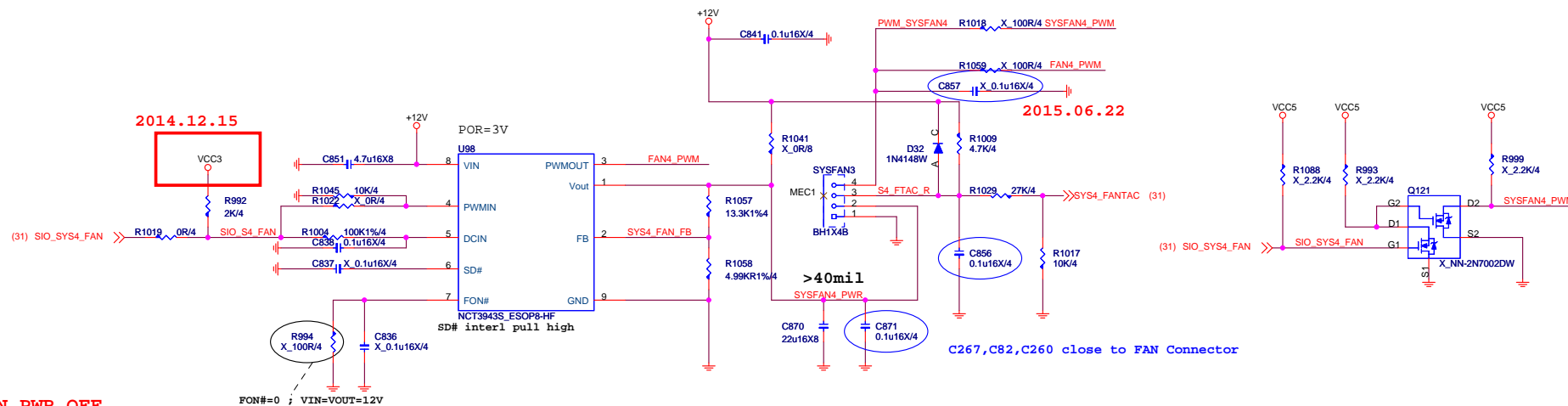
Type H : 4/3 PIN SYS FAN FROM NCT3943S(USE SIO CUT POWER)

PUMPFAN



Type H : 4/3 PIN SYS FAN FROM NCT3943S(USE SIO CUT POWER)

SYSFAN3



SYSFAN_PWR_OFF
SIO control
Close SIO_SYS1_FAN Vout=0

OPTFAN1



OPTFAN2

(17.45) PCH_SPI_MOSI <<PCH_SPI_MOSI

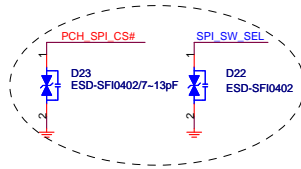
(17.45) PCH_SPI_MISO <<PCH_SPI_MISO

(17.45) PCH_SPI_CLK <<PCH_SPI_CLK

(17) PCH_SPI_IO2 <<PCH_SPI_IO2

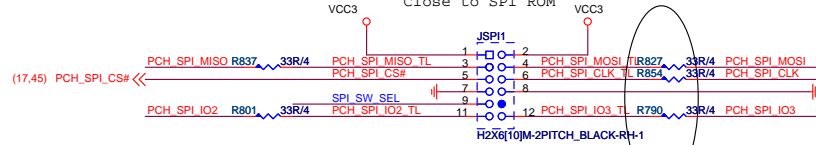
(17) PCH_SPI_IO3 <<PCH_SPI_IO3

For T1624 1.1: stuff D19
Old: Unstuff due to 12V



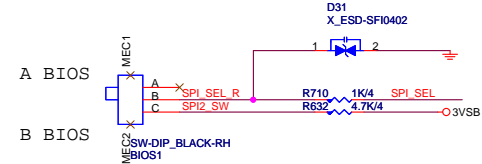
SPI DEBUG PROT

Close to SPI ROM



For T1624 1.1: Stuff R1232
Old: Unstuff

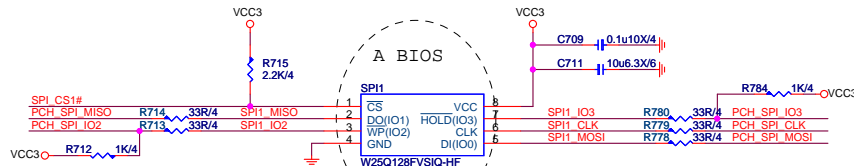
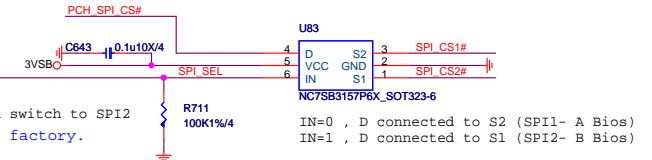
Part Number: N31-2061341-H06



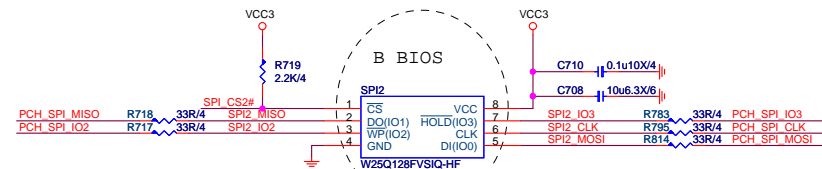
SIO NCT6793 GP71

(31) SPI_SEL >>

GPI default low
Active push pull high switch to SPI2
For auto testing in factory.



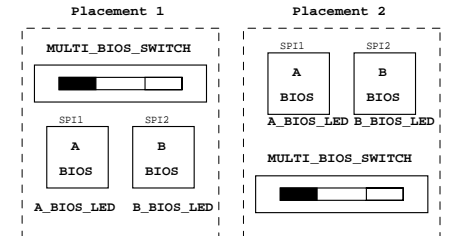
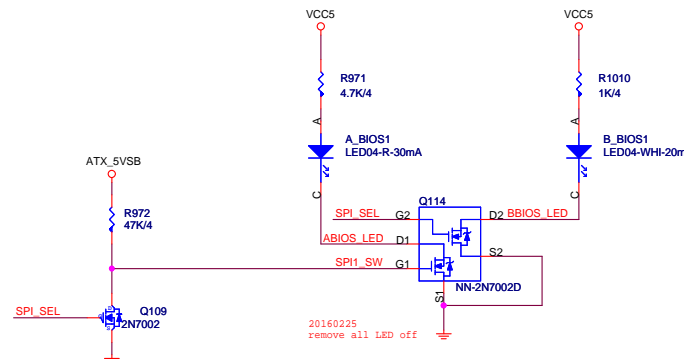
16M ROM



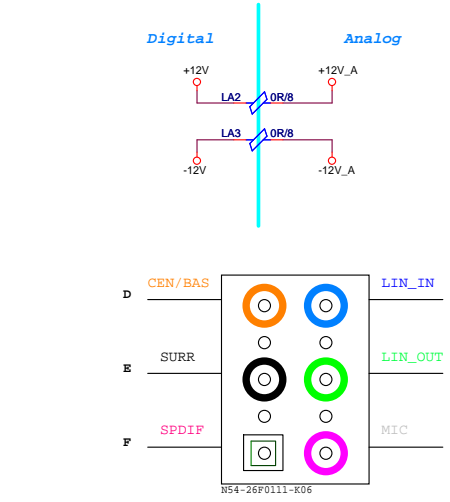
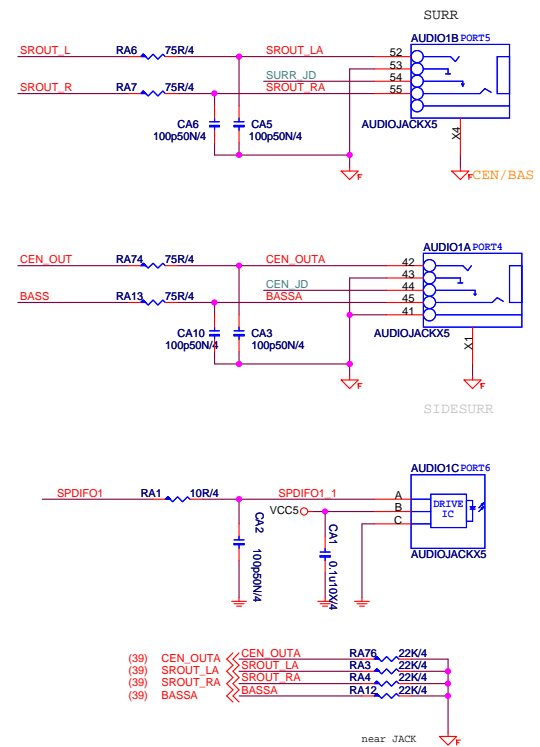
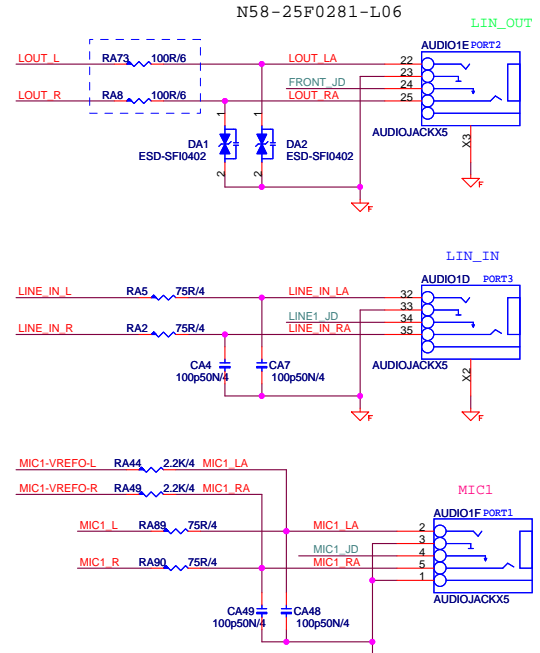
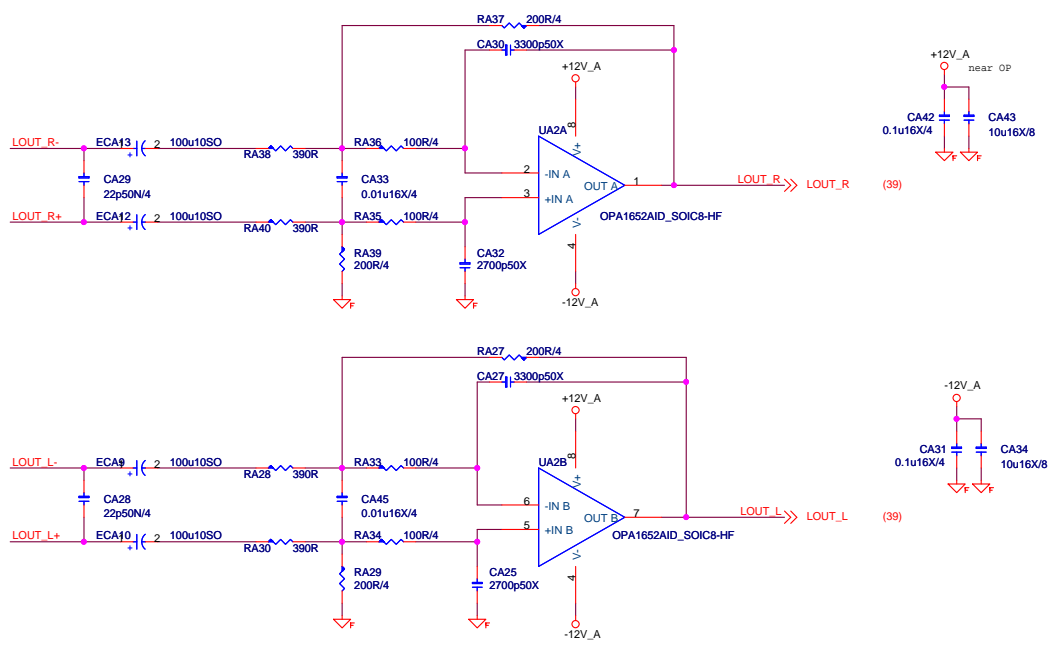
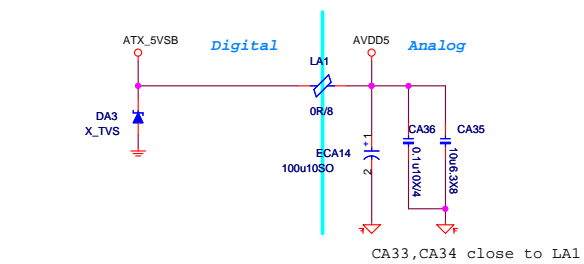
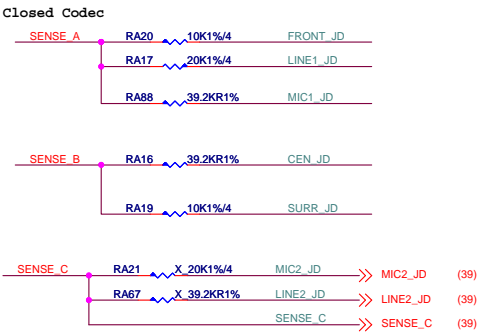
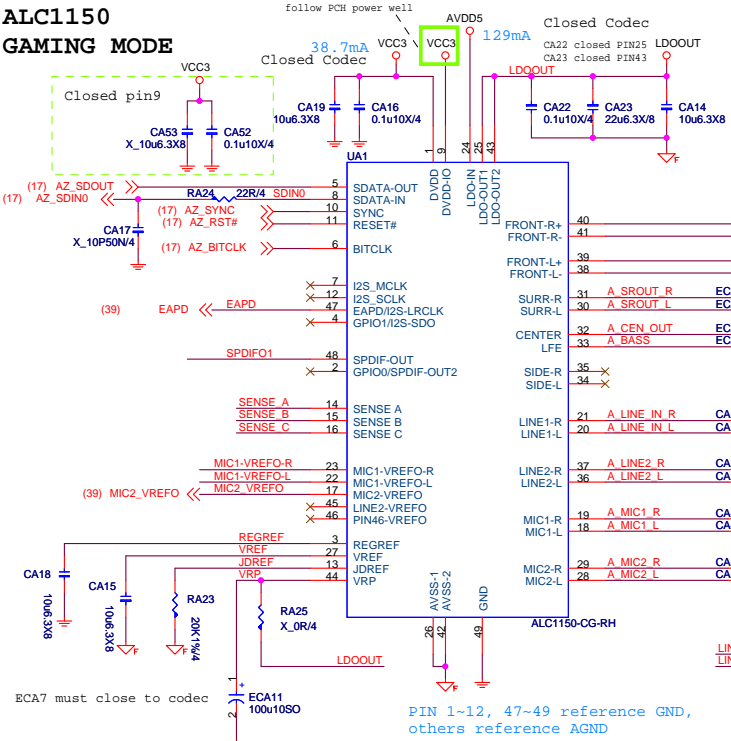
SPI FLASH ROM

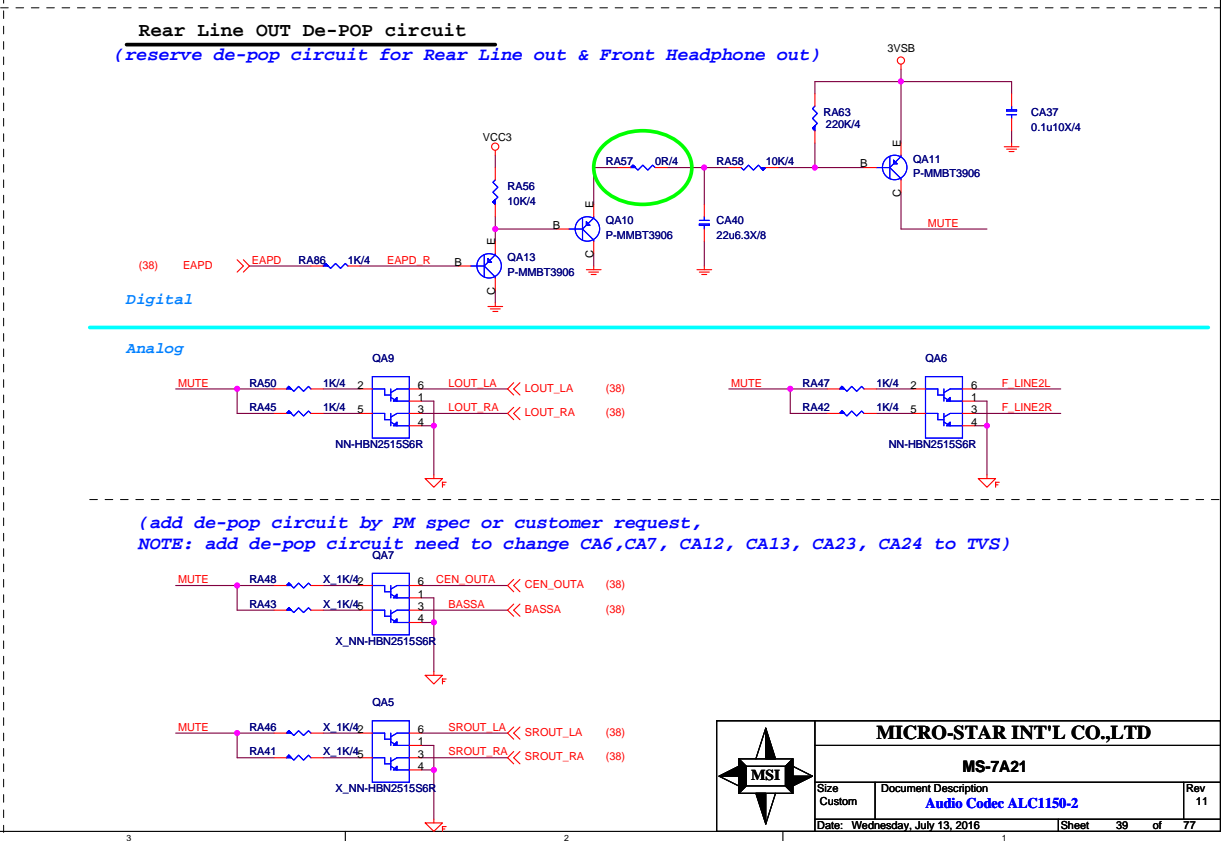
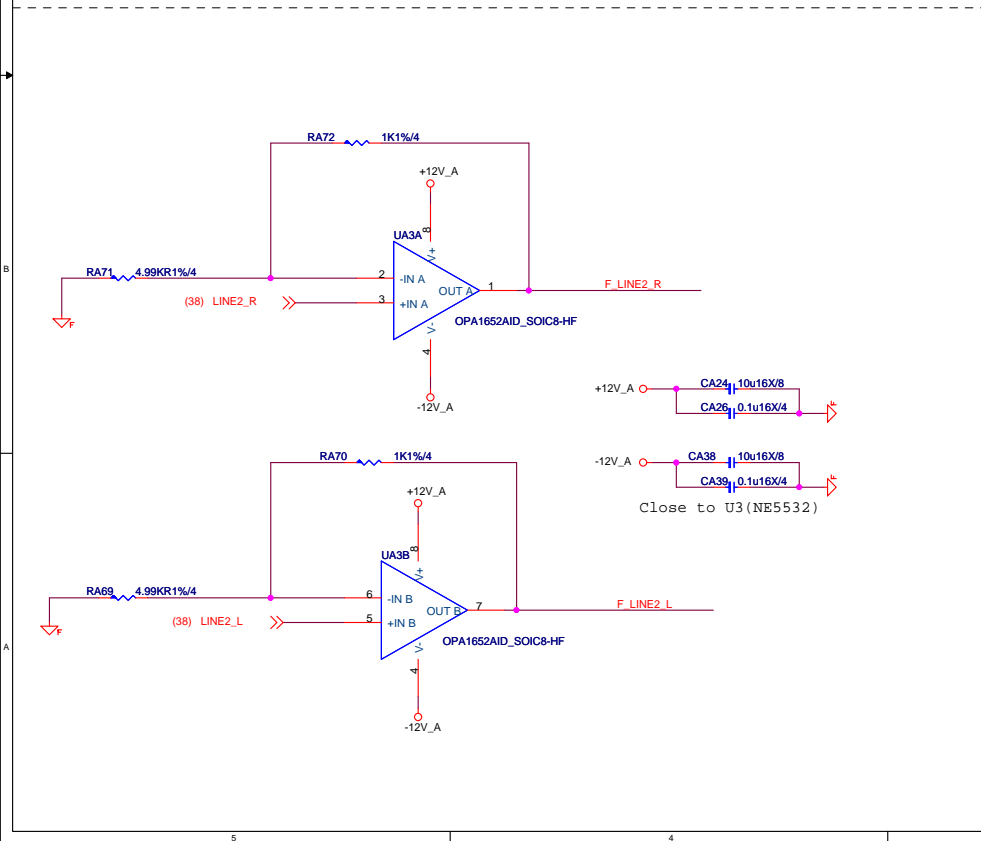
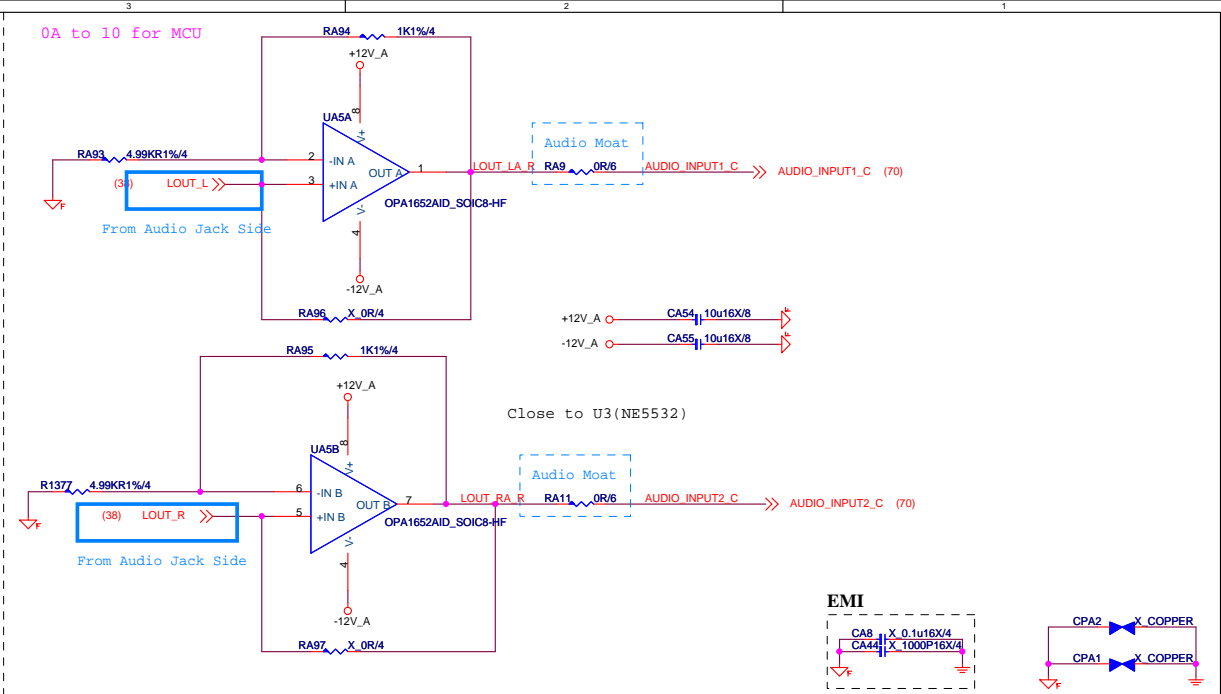
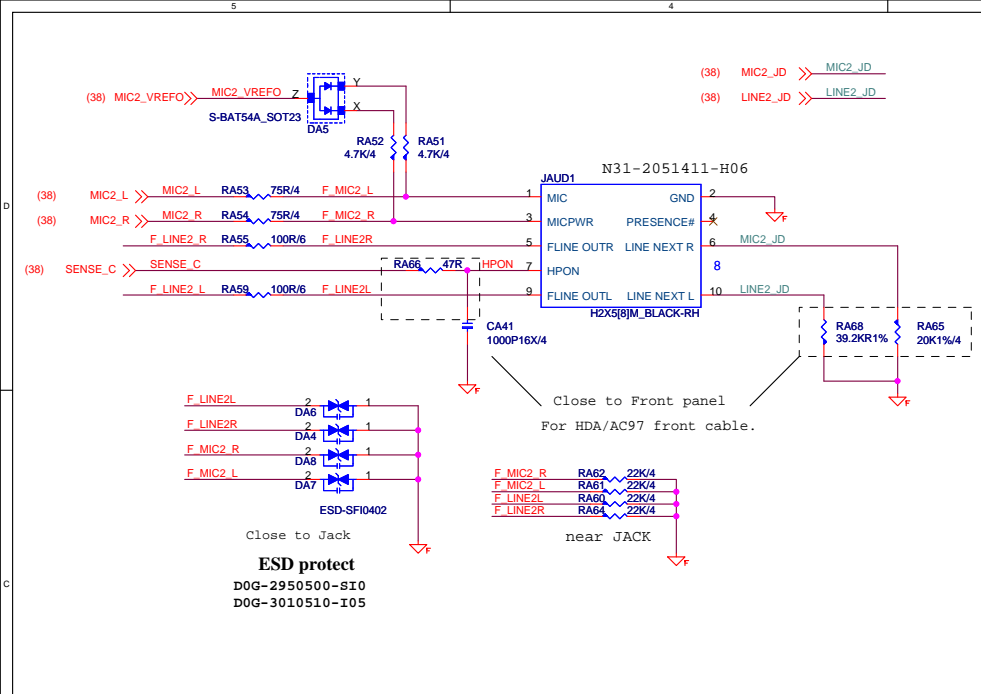
Place close to SB.

*SPI_CLK & SPI_MOSI must be length matched to within 500mils.
*SPI_CLK & SPI_CS# must be length matched to within 500mils.

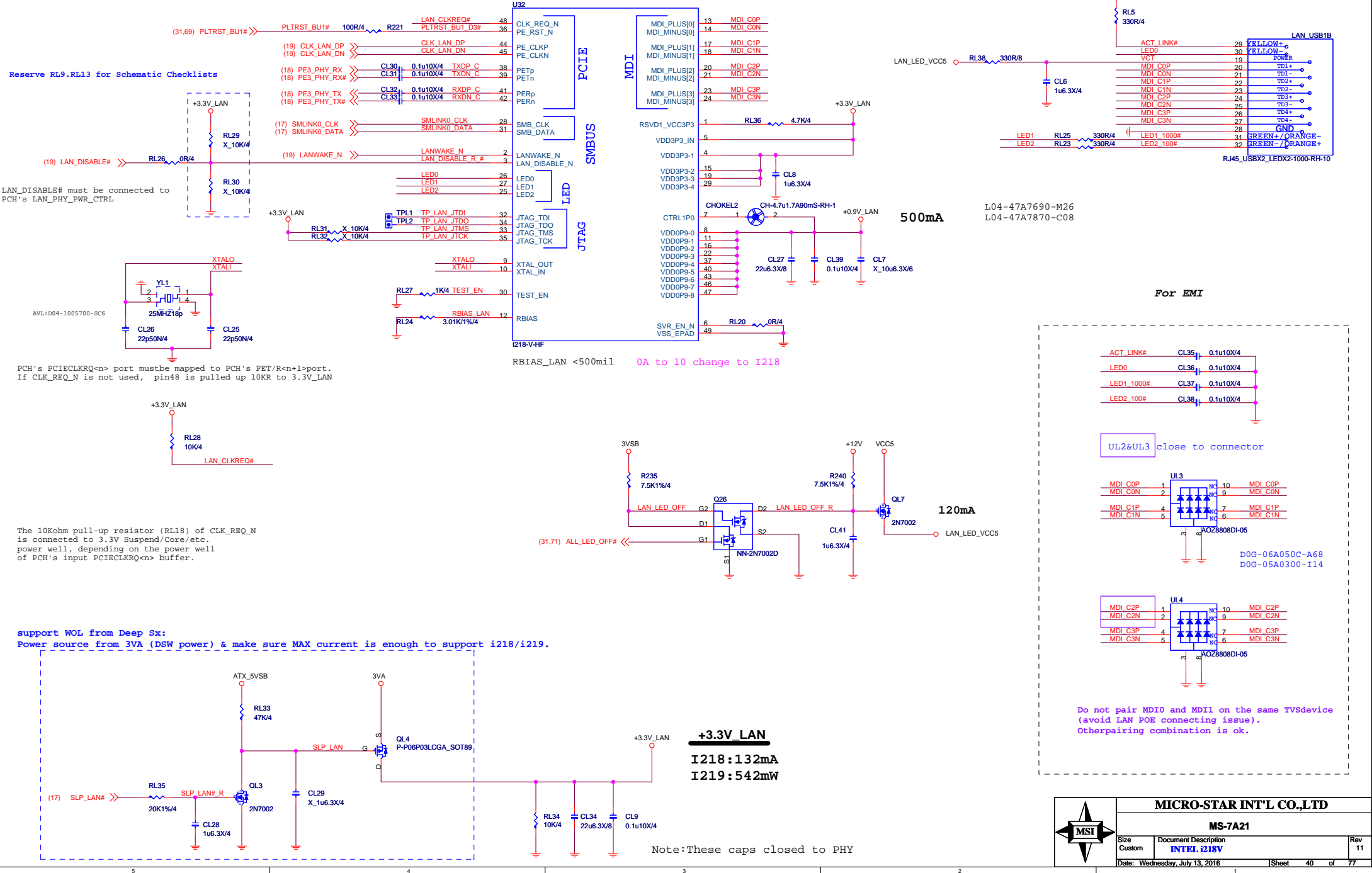


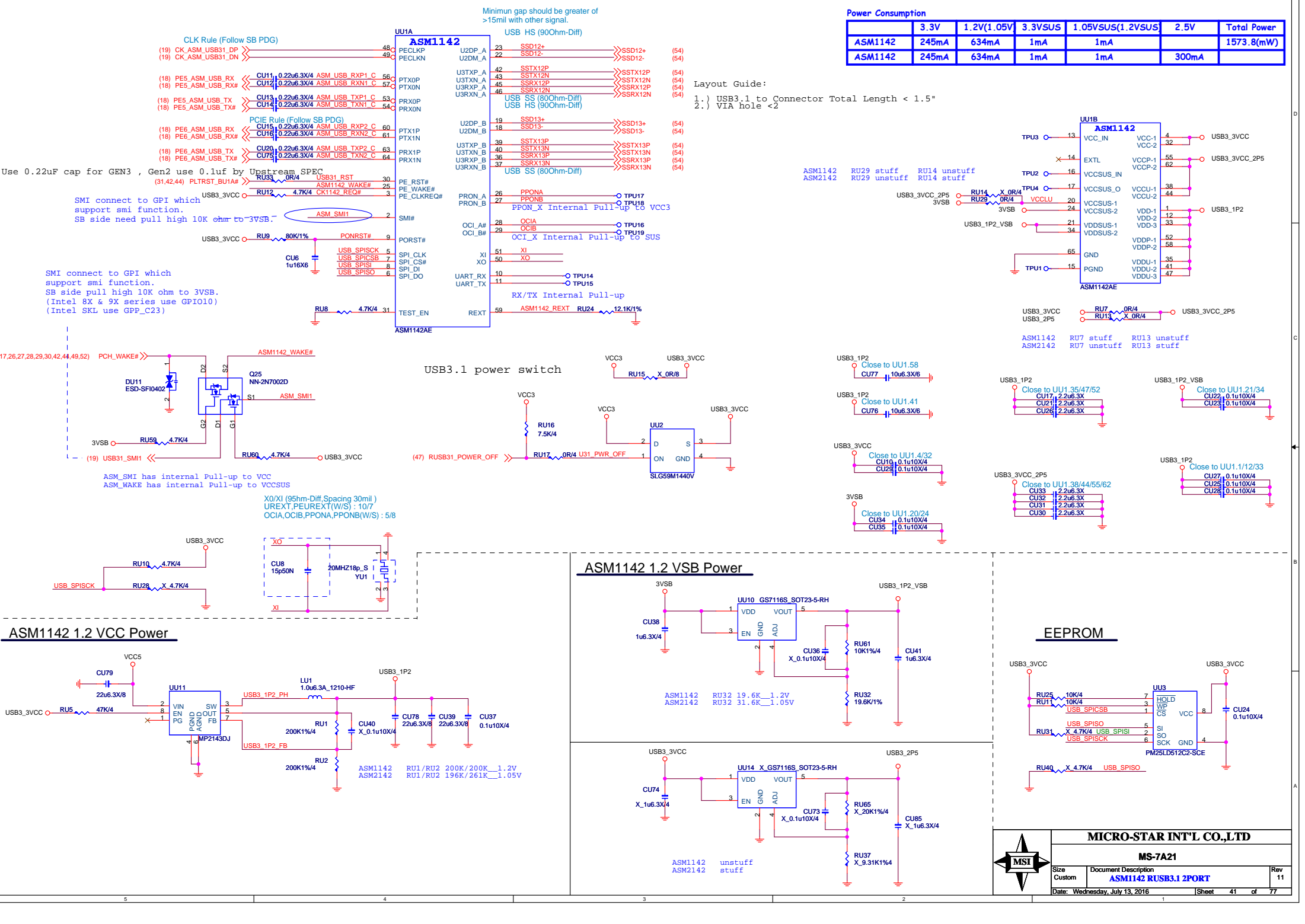
MICRO-STAR INT'L CO.,LTD			
MS-7A21			
Size	Document Description	Rev	
Custom	Dual BIOS	11	
Date: Wednesday, July 13, 2016		Sheet	37 of 77





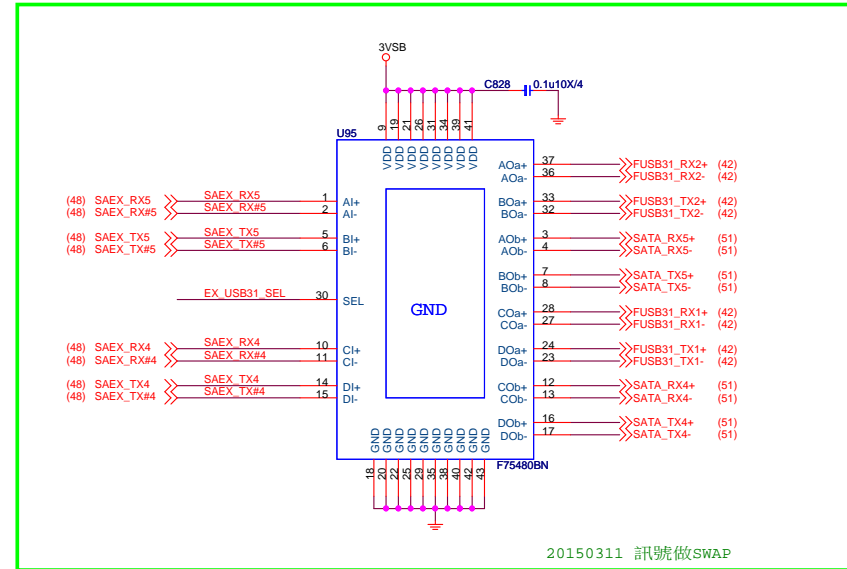
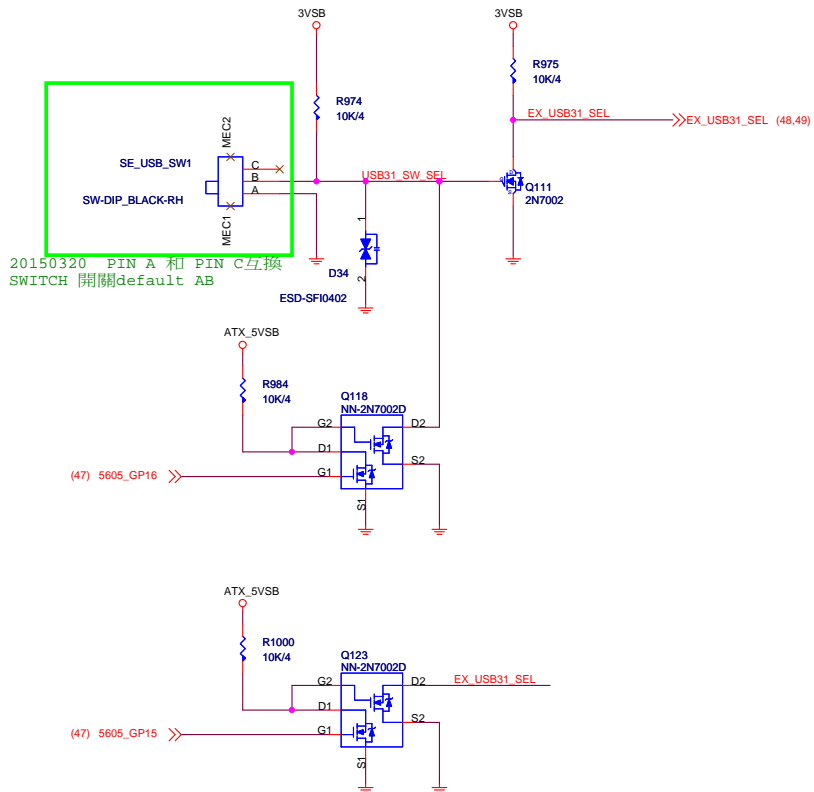
Intel I219V / I218V PHY





確認一下default 是否為BC

增加一個GPIO給BIOS判斷為PCIE或SATAEXPRESS



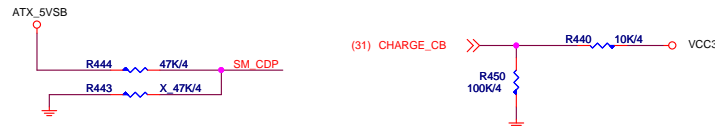
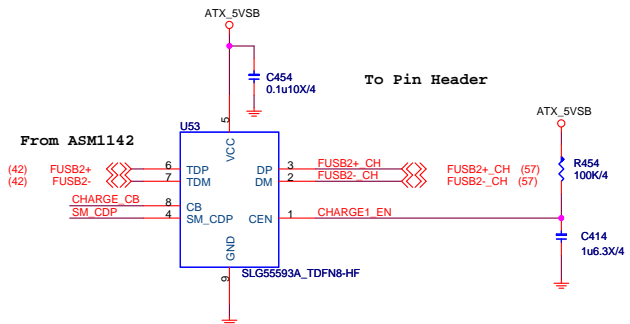
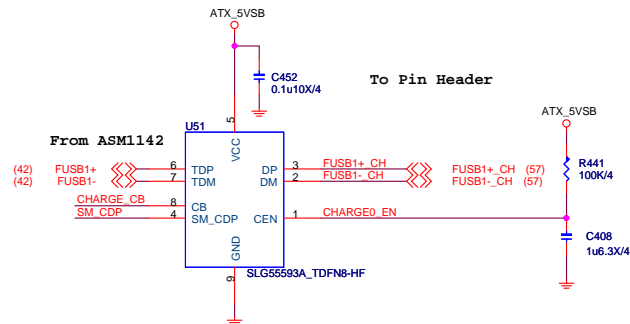
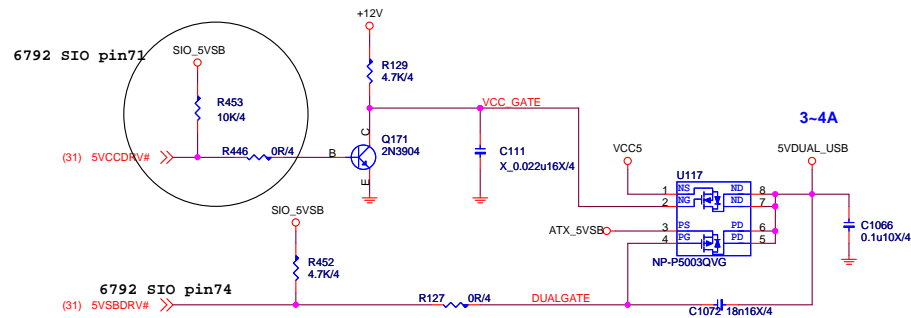
BIOS_MODE

5605_GP16	5605_GP15	SEL	Mode
1	1	SATA	default
0	1	SATA	
0	0	USB3.1	

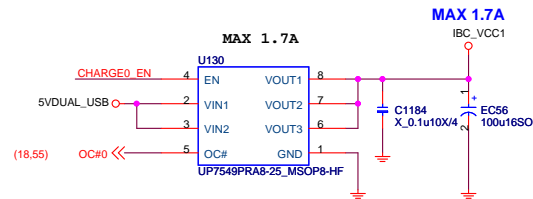
Switch_MODE

Switch	SEL	Mode	
A_B	SATA		
B_C	USB3.1	default	

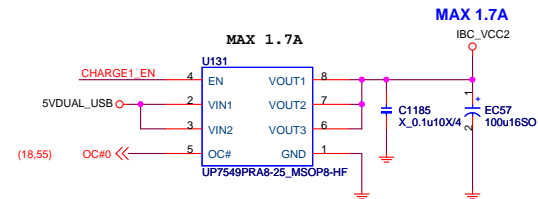
0A to 10 change to jusb4 19 pin use.

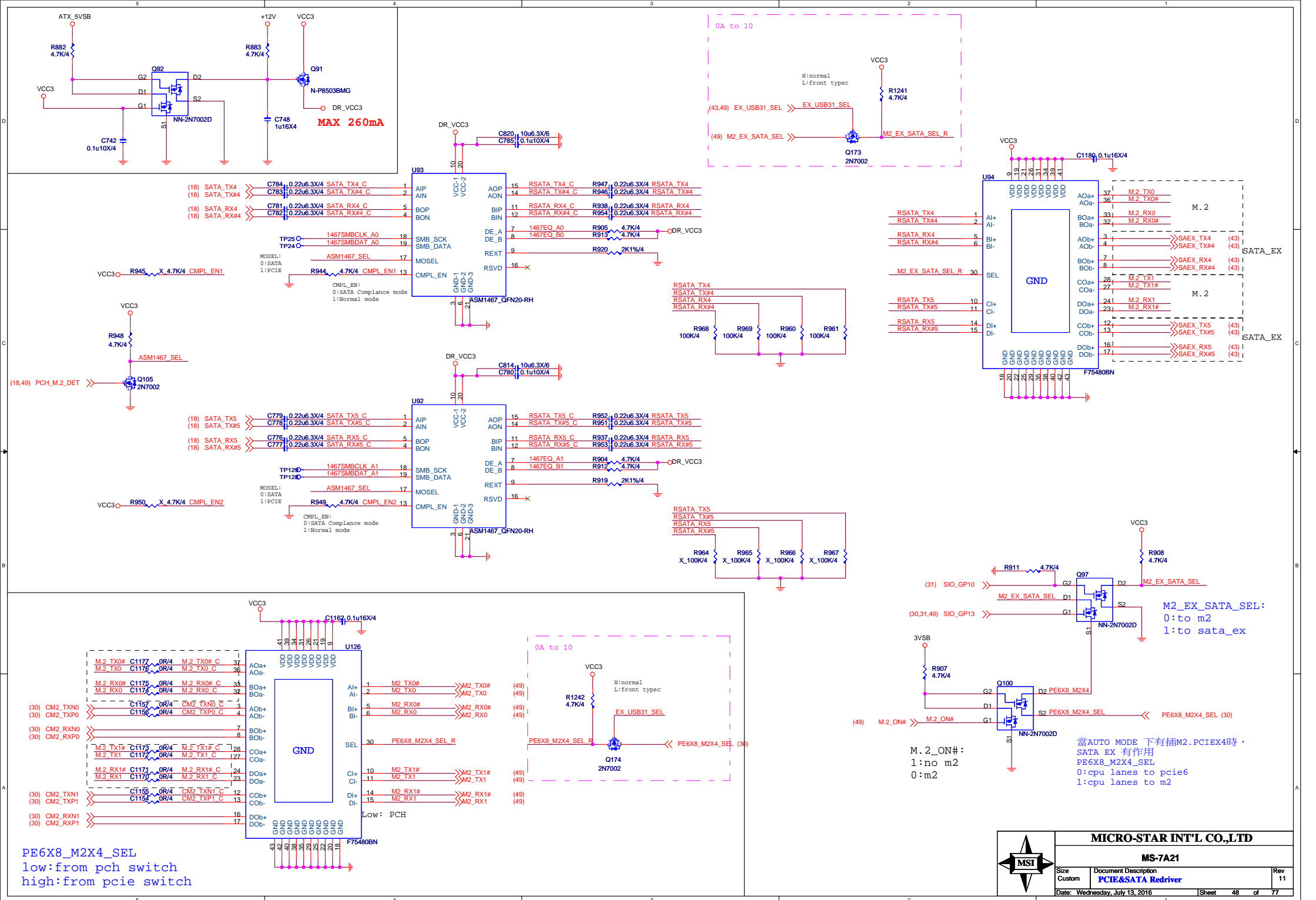


USB POWER PORT 1 For USB Charging



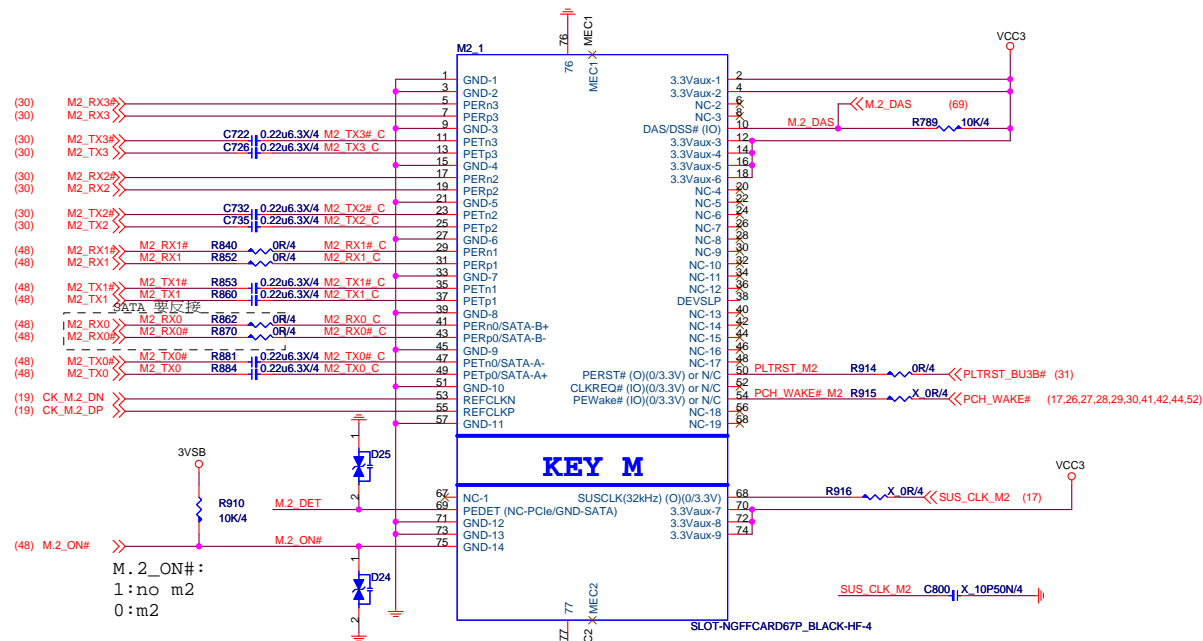
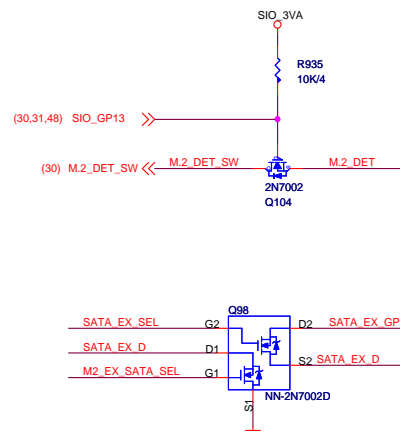
USB POWER PORT 1 For USB Charging





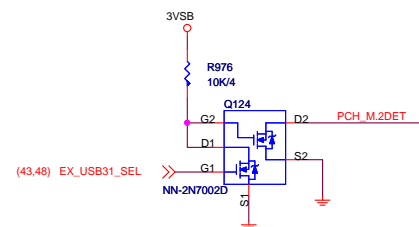
BIOS_MODE

SIO_GP10	SIO_GP80	SIO_GP84	SIO_GP13	Mode
1	0	1:PCIE 0:SATA	0	M2-PCH
X	1	X	0	PCIEX8
X	0	X	0	M2-X4
0	X	1:PCIE 0:SATA	X	SATA Express
GPI	GPI	GPI	1	AUTO



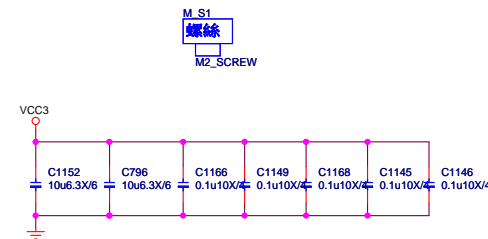
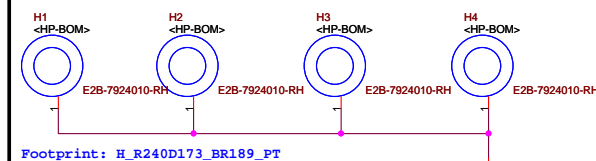
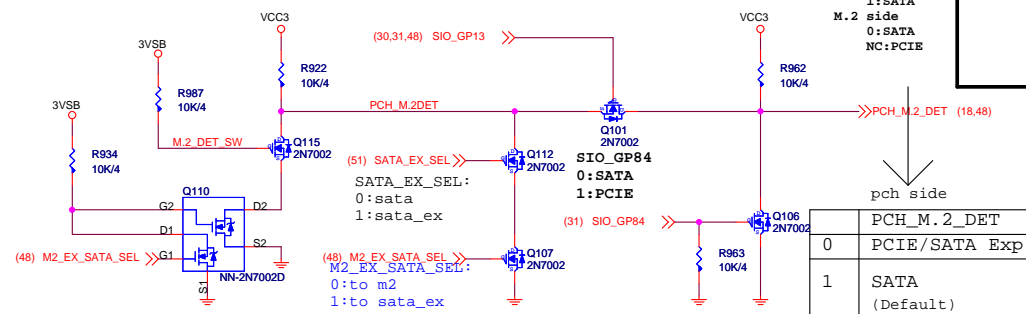
Socket3(B+M) : support up to PCIex4 / SSD
(Support dimension: Type 2242 / Type 2260 / Type 2280)

FRONT_U3.0 SEL



BIOS_MODE SATA & PCIE SWITCH

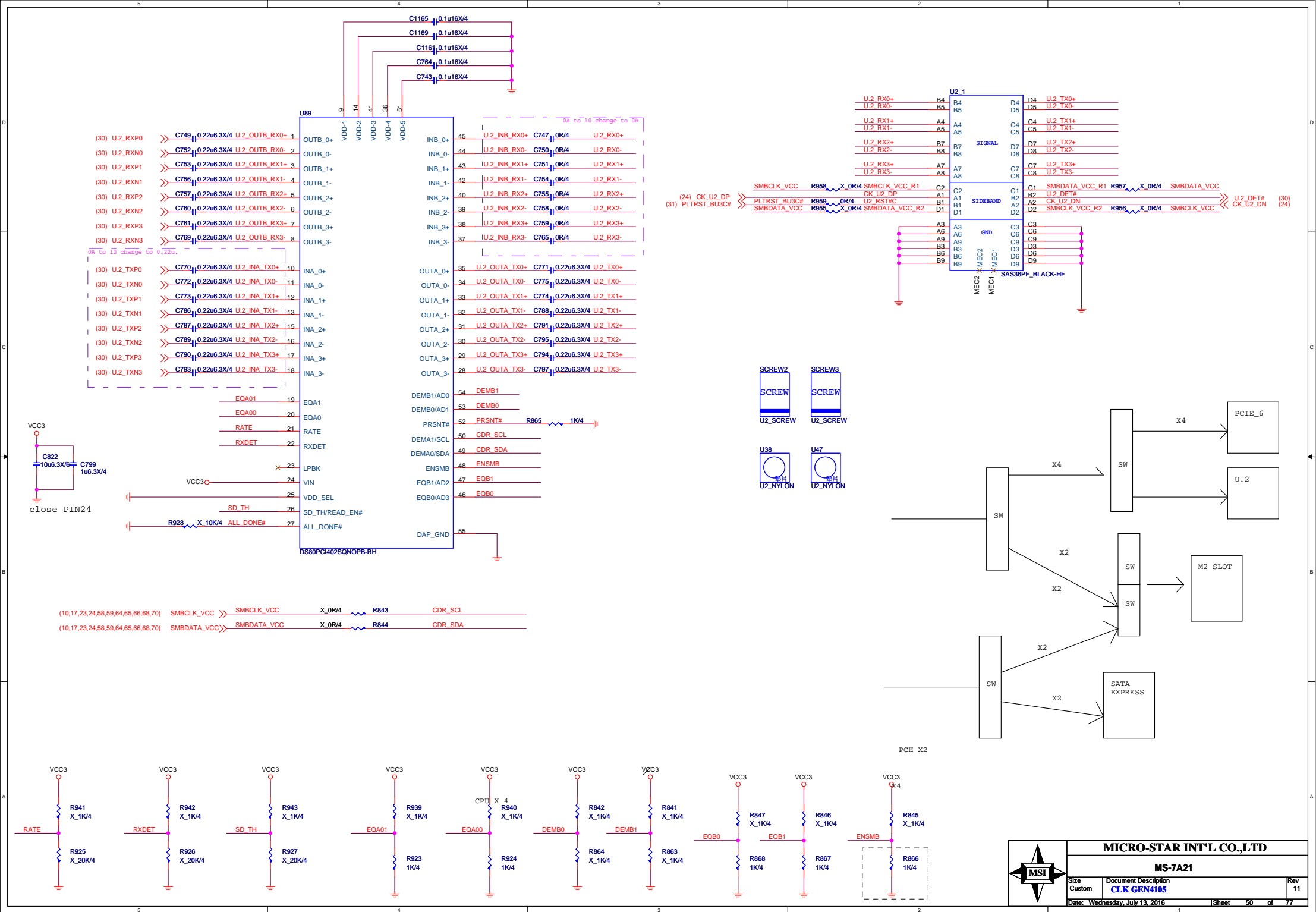
GP13	GP80	GP11	GP10	GP84	Mode
1	0	0	0	0	AUTO(Default)
0	X	1	1	0	M2-SATA
0	X	1	1	1	M2-PCIE
0	0	0	X	X	M2-CPU
0	X	X	0	0	SATA-E SATA
0	X	X	0	1	SATA-E PCIE



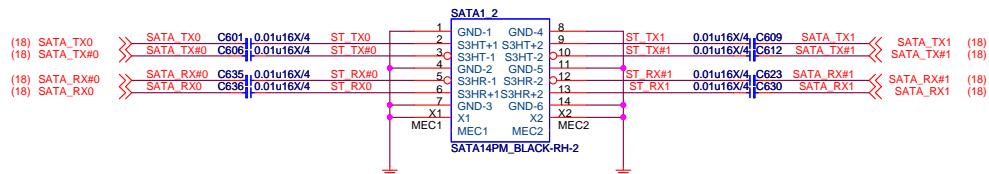
MICRO-STAR INT'L CO.,LTD

MS-7A21

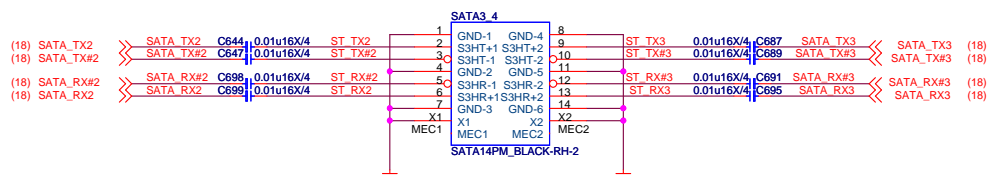
Size Custom	Document Description M.2 CONNECTOR	Rev 11
Date: Wednesday, July 13, 2016		Sheet 49 of 77



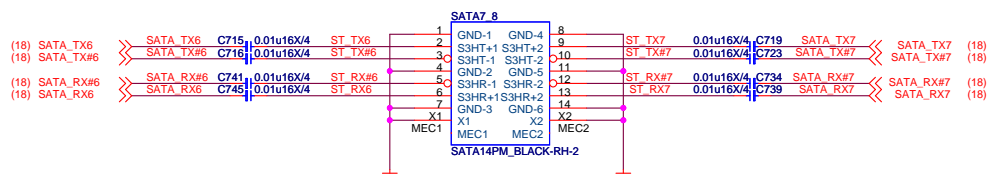
SATA 6G PORT 0.1



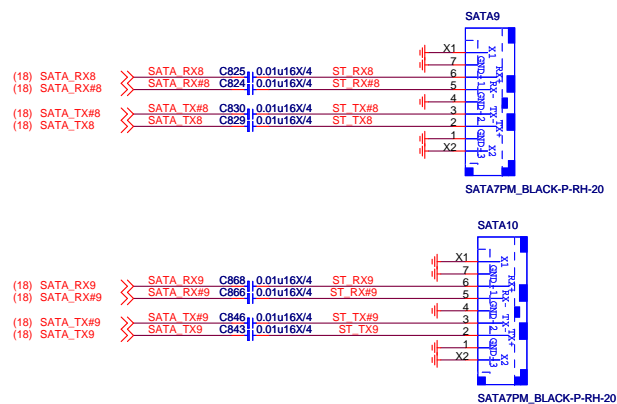
SATA 6G PORT 2.3



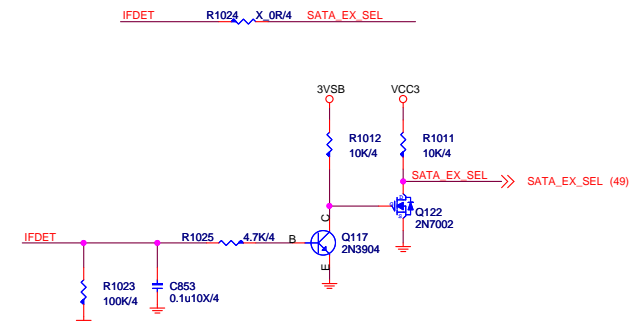
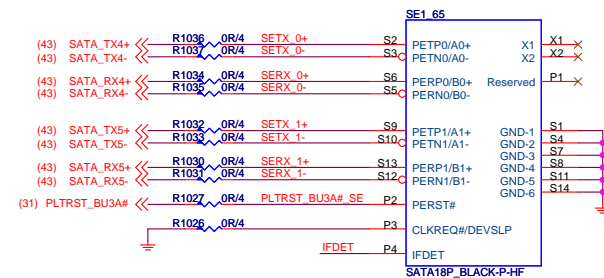
SATA 6G PORT 6.7



SATA 6G PORT 8.9



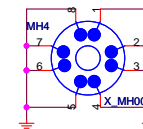
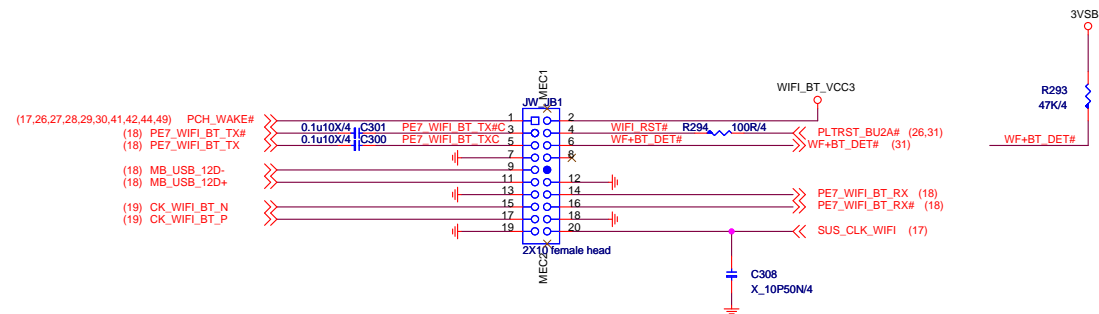
SATA 6G PORT 56



MICRO-STAR INT'L CO.,LTD

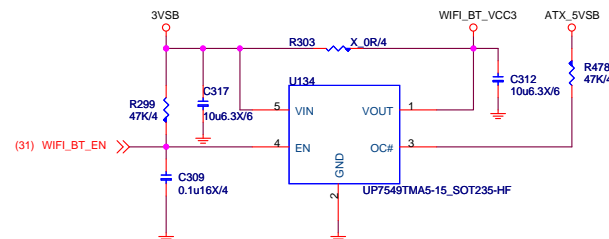
MS-7A21

Size Custom	Document Description SATA Connector	Rev 11
Date: Wednesday, July 13, 2016		Sheet 51 of 77



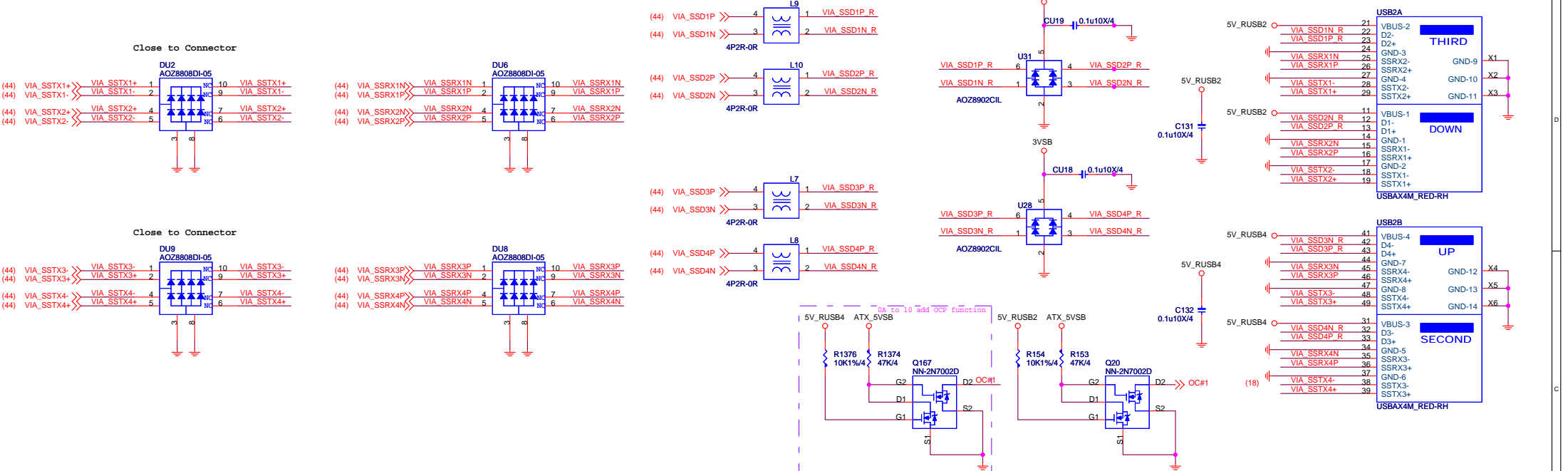
VIRTU_LA8
Label
VIRTU
WIFI

VIRTU_LA9
Label
VIRTU
WIFI_SCREW

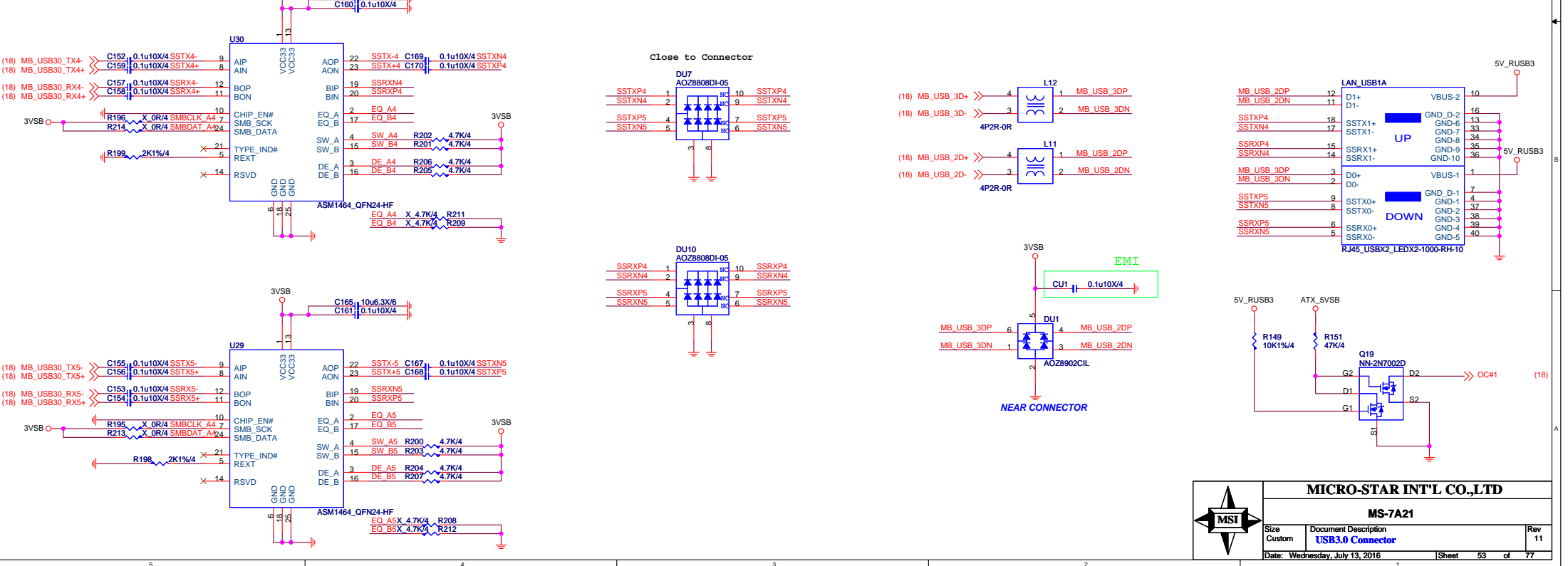


MICRO-STAR INT'L CO.,LTD		
MS-7A21		
Size Custom	Document Description WIFI+BTconnector	Rev 11
Date: Wednesday, July 13, 2016		Sheet 52 of 77

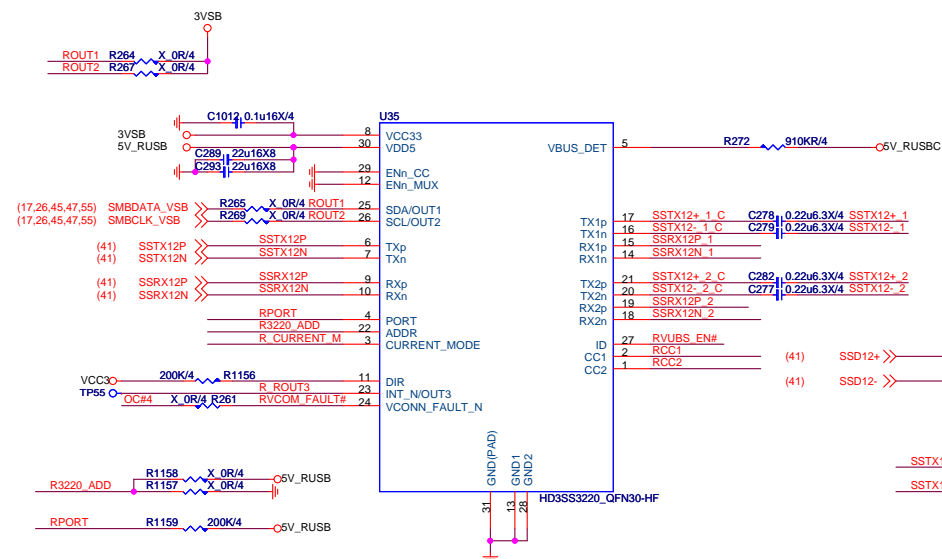
REAR USB3.0 Connector



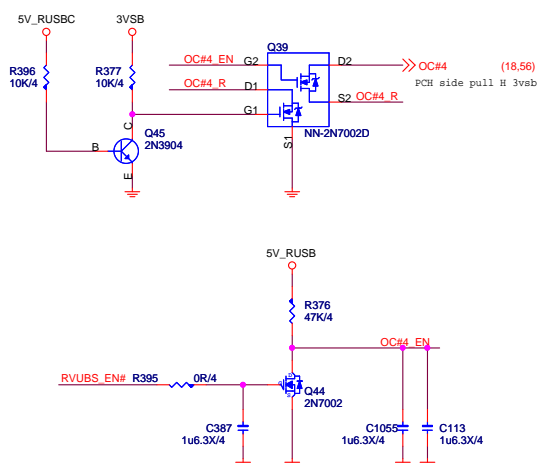
LAN USB3.0



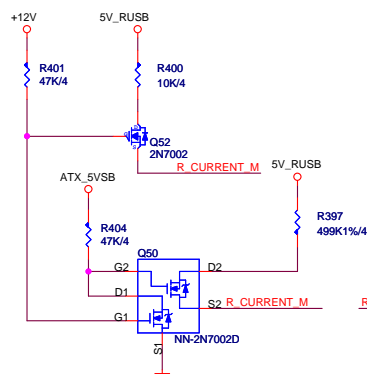
USB3.1



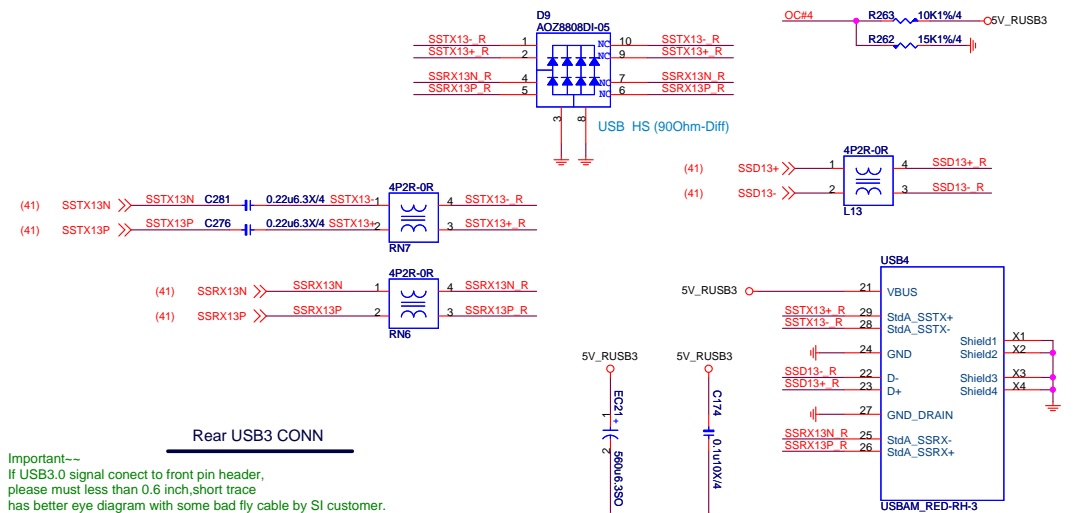
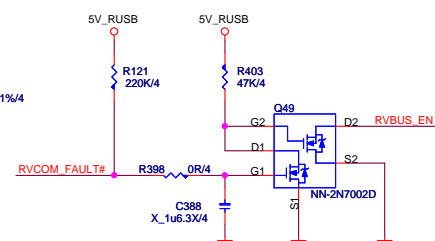
USB OC# Singal



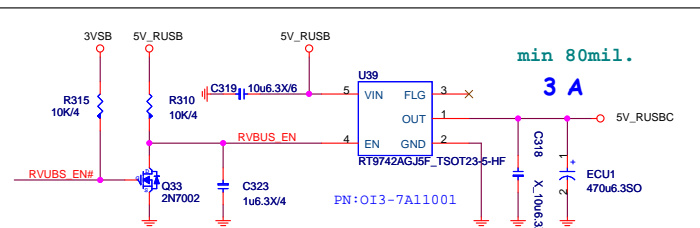
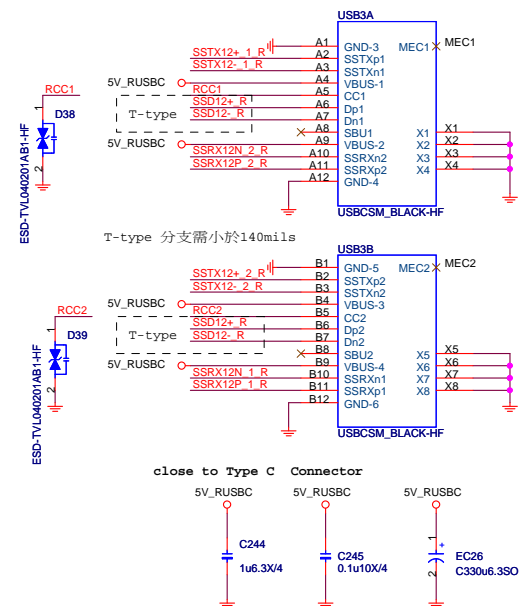
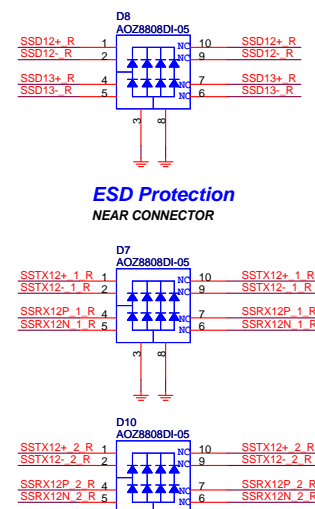
Current Mode



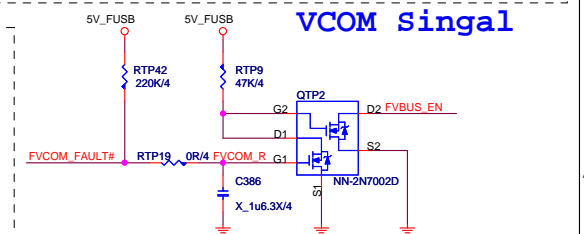
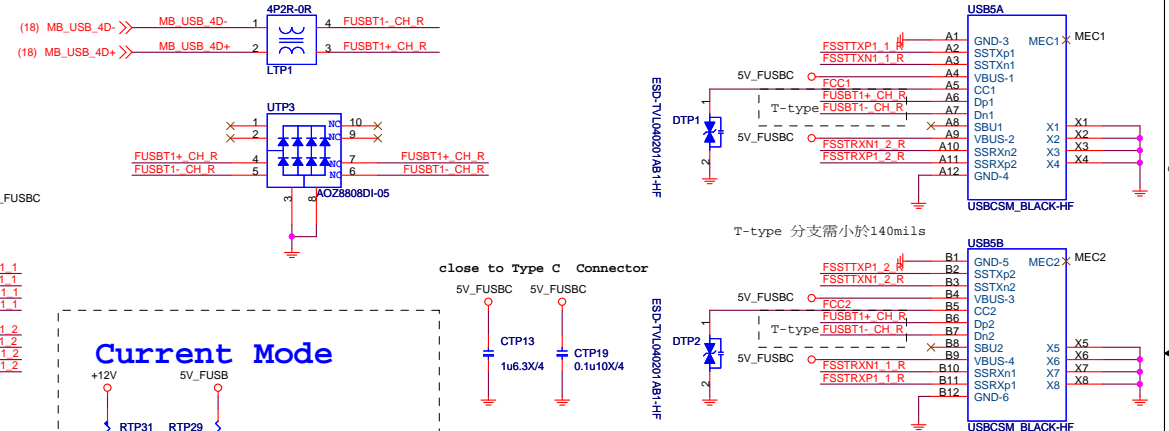
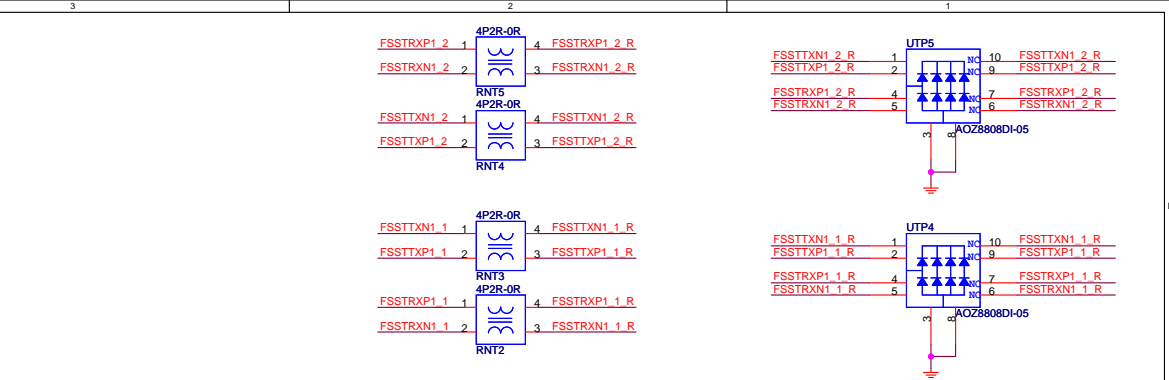
VCOM Singal



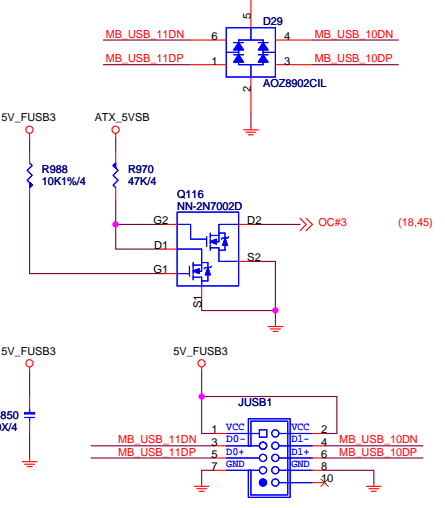
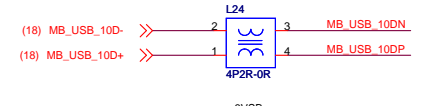
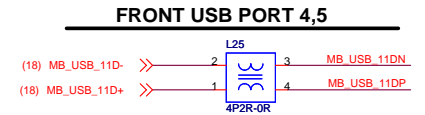
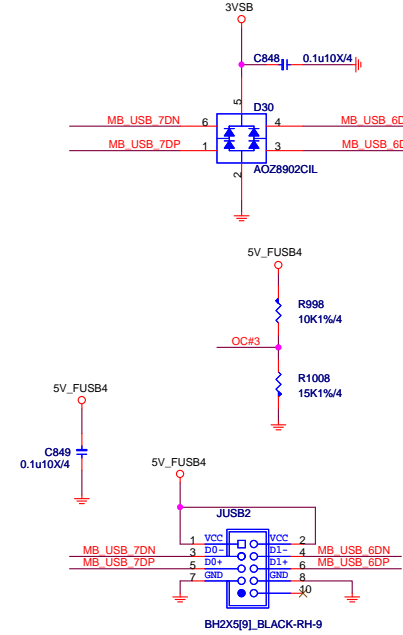
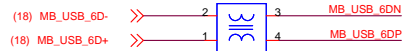
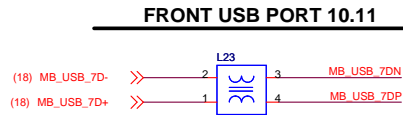
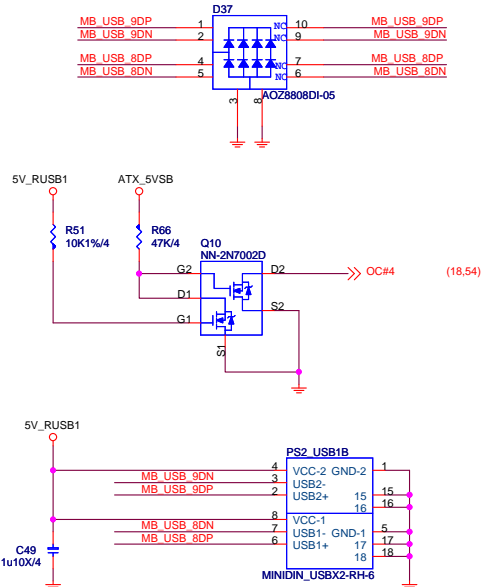
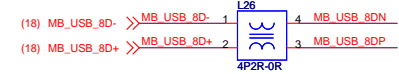
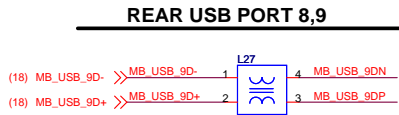
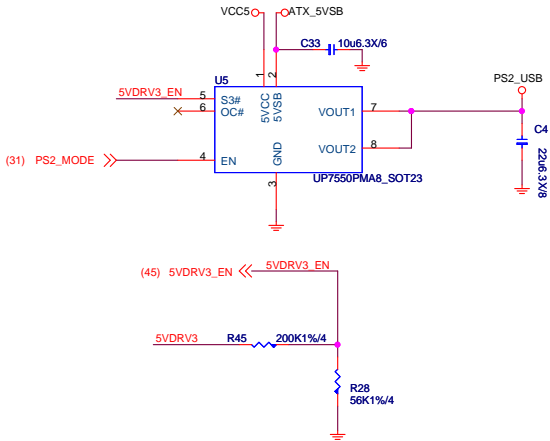
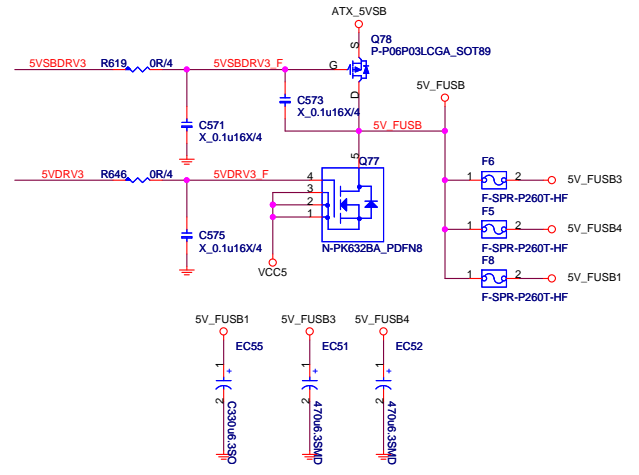
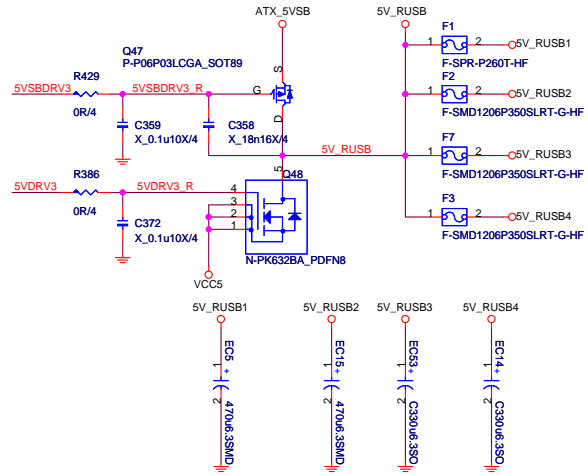
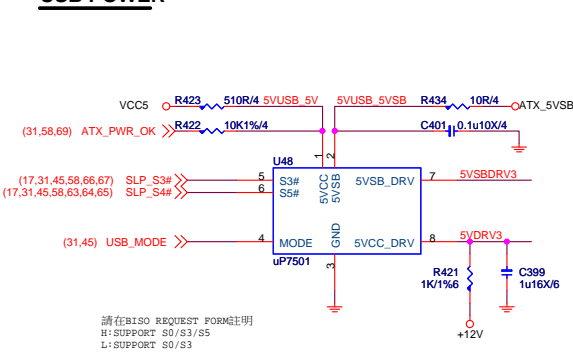
ESD Protection
NEAR CONNECTOR



MICRO-STAR INT'L CO.,LTD			
MS-7A21			
Size Custom	Document Description USB3.1 REAR TYPE-A+C CONN		Rev 11
Date: Wednesday, July 13, 2016		Sheet 54	of 77



USB POWER



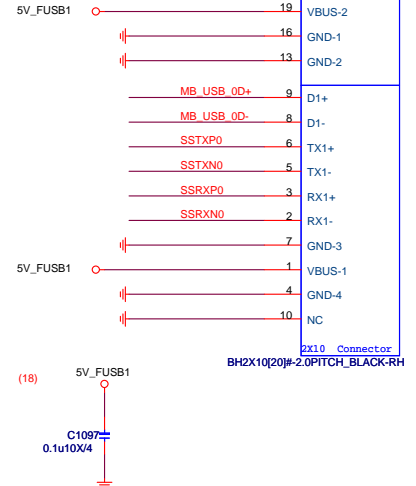
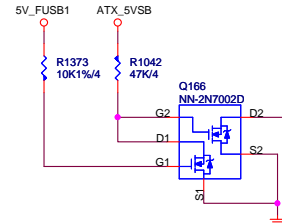
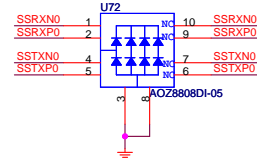
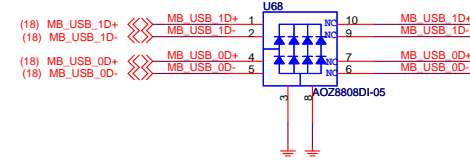
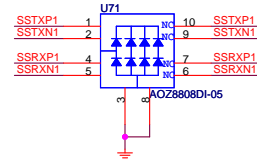
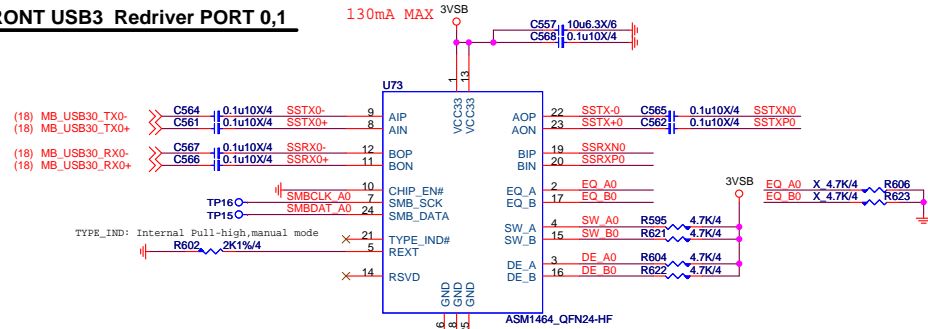
MICRO-STAR INT'L CO.,LTD

MS-7A21

Size Custom	Document Description Rear/Front USB2.0	Rev 11
Date: Wednesday, July 13, 2016		Sheet 56 of 77

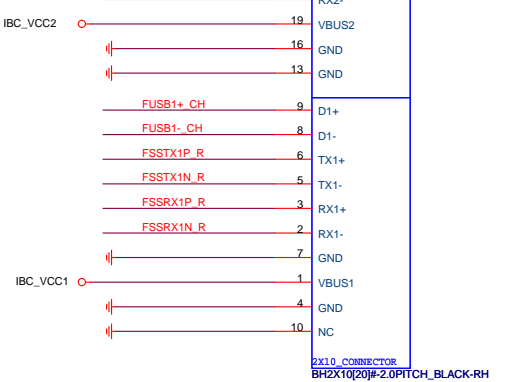
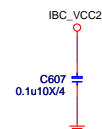
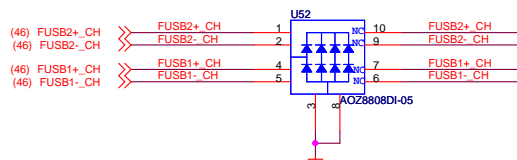
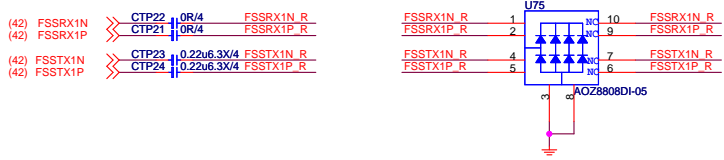
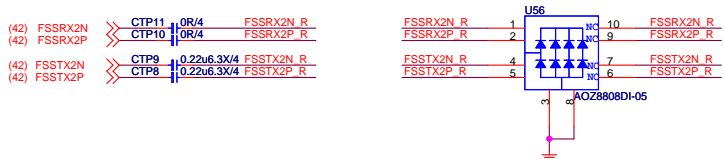
FRONT USB3 Redriver PORT 0,1


130mA MAX



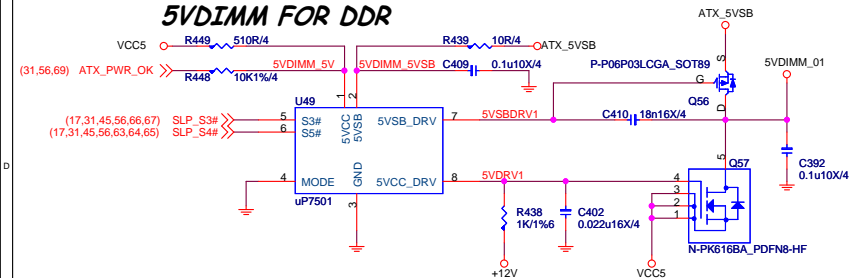
FRONT USB3 Redriver PORT 2,3

0A to 10



	MICRO-STAR INT'L CO.,LTD		
	MS-7A21		
	Size	Document Description	Rev
	Custom	FRONT USB REDRIVER CONNECTOR	11
	Date: Wednesday, July 13, 2016	Sheet 57 of 77	

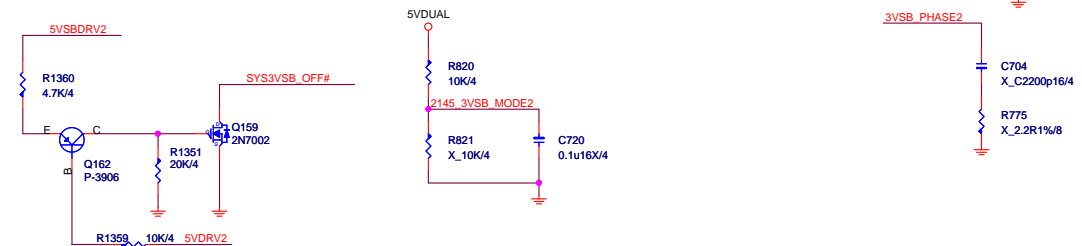
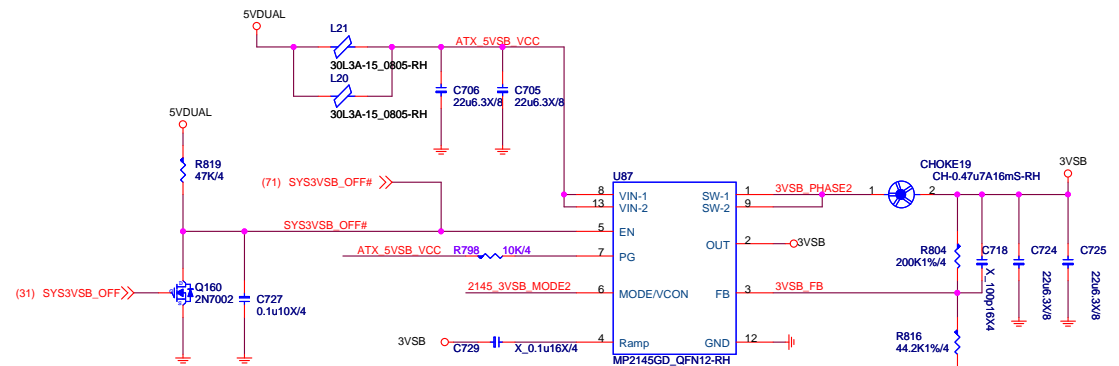
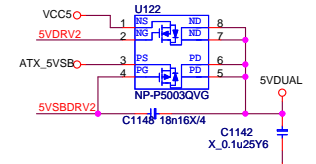
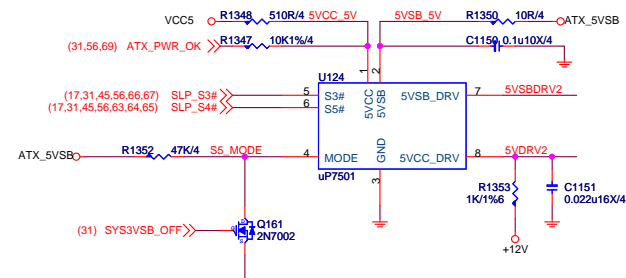
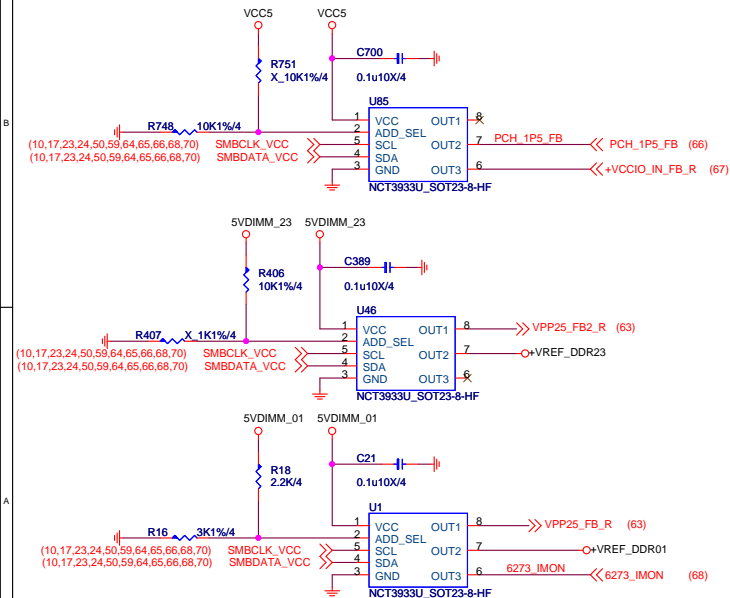
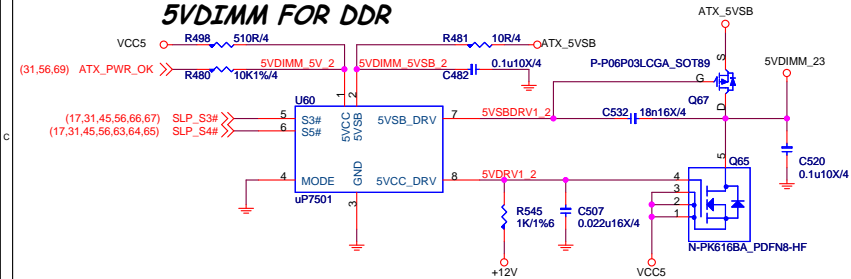
5VDIMM FOR DDR



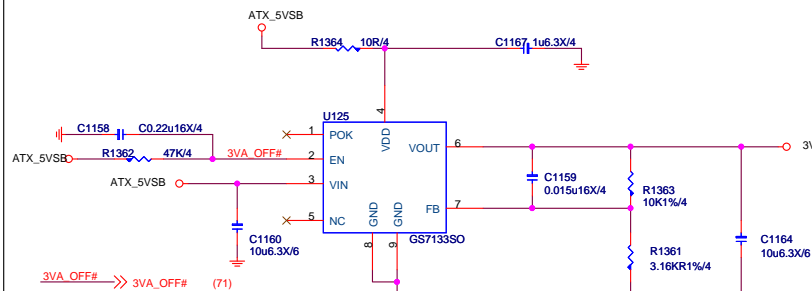
7501 Mode
H:Support S0/S3/S5
L:Support S0/S3

5VDRV1看VCC5起來6~10ms後起來,因為當初挑power

5VDIMM FOR DDR

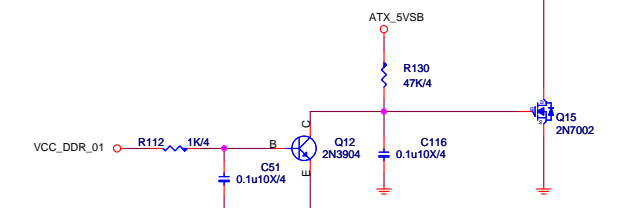
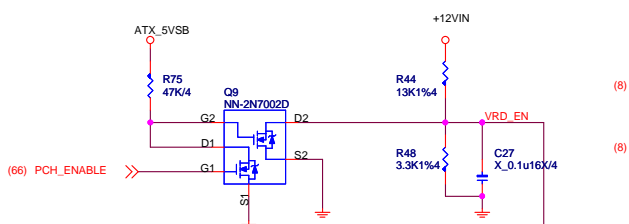
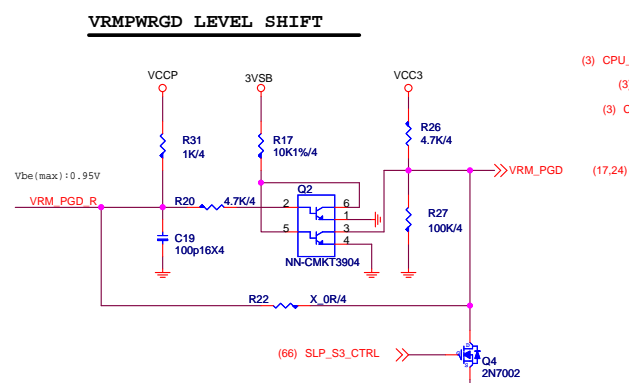


防G3-->S5底下5VSBDRV2瞬間有電變沒電,使得下一級電壓爬升有drop



MSI			
MICRO-STAR INT'L CO.,LTD			
MS-7A21			
Size	Document Description	Rev	
Custom	ACPI controller UPI	11	
Date: Wednesday, July 13, 2016		Sheet	58 of 77

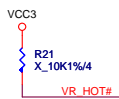
VRMPWRGD LEVEL SHIFT



close to VRM

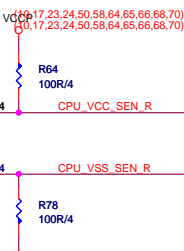
(3) CPU_SVID_ALERT_N >> CPU_SVID_ALERT_N R1086 X 56R/4
(3) CPU_SVID_CLK >> CPU_SVID_CLK R1085 56R/4
(3) CPU_SVID_DATA >> CPU_SVID_DATA R1087 100R/4

between 3 to 6 inches

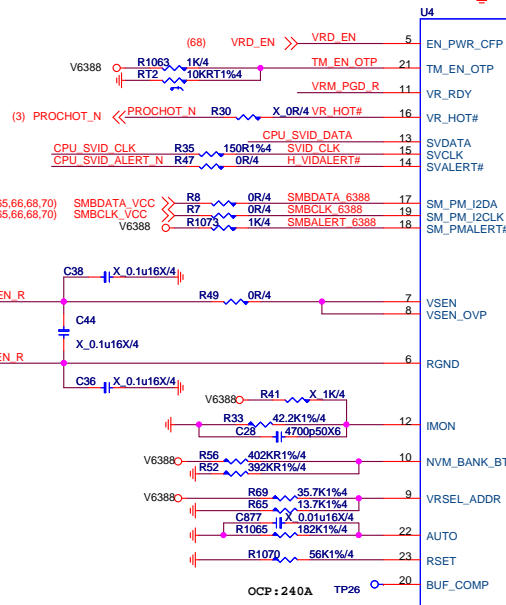
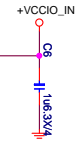
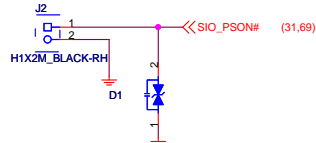
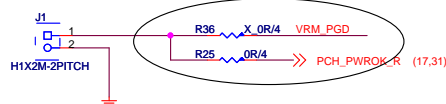


(8) CPU_VCC_SENSE >> VR73 0R/4

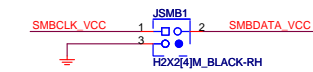
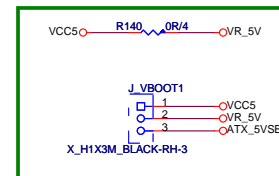
(8) CPU_VSS_SENSE >> R105 0R/4

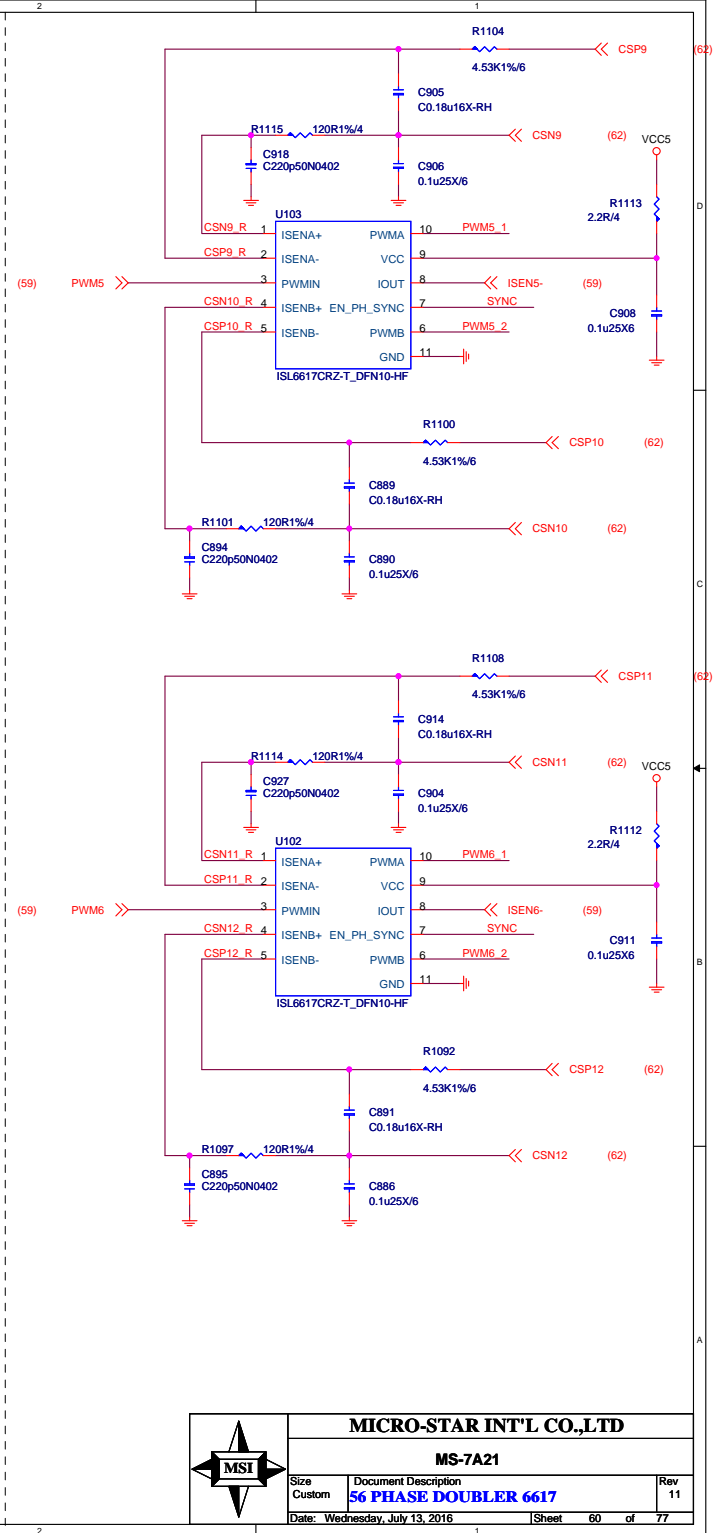
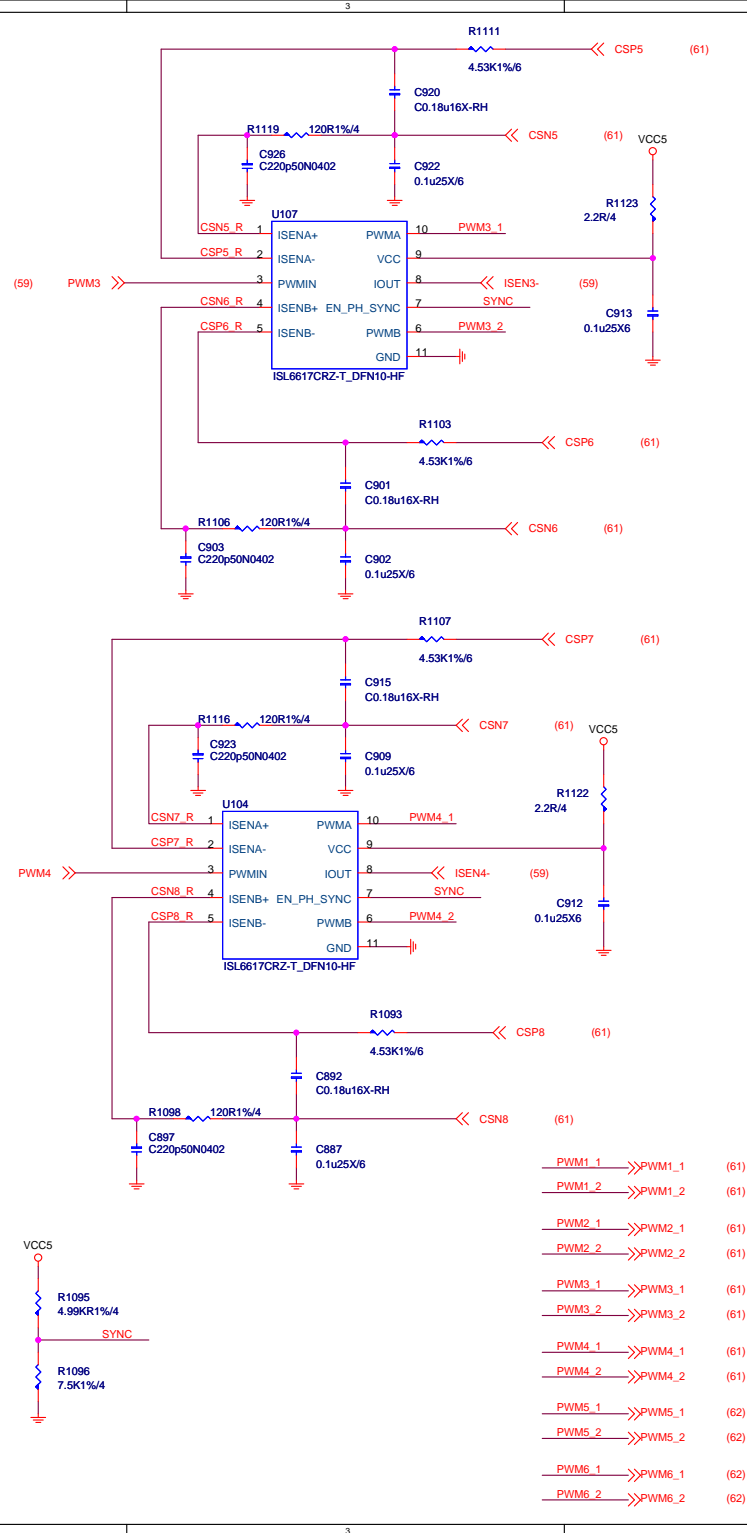
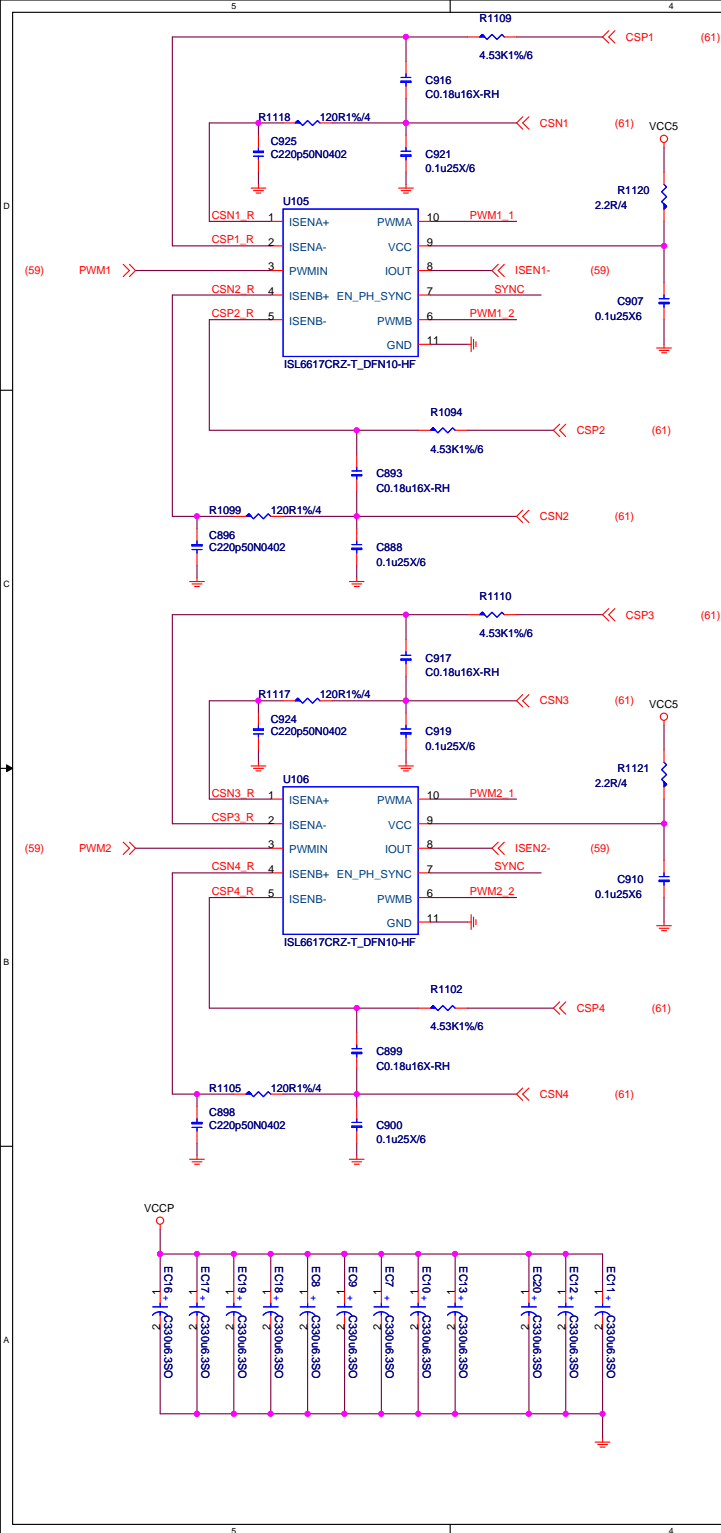


(240A / 12 Phase) * DCR / (Risen + Rset/64)
= 100uA
R753=4.64k ohm



ISL6388HRTZ-T_T0FN40-HF-6
close phase sequence 6-3-5-2-4-1
address:8AH

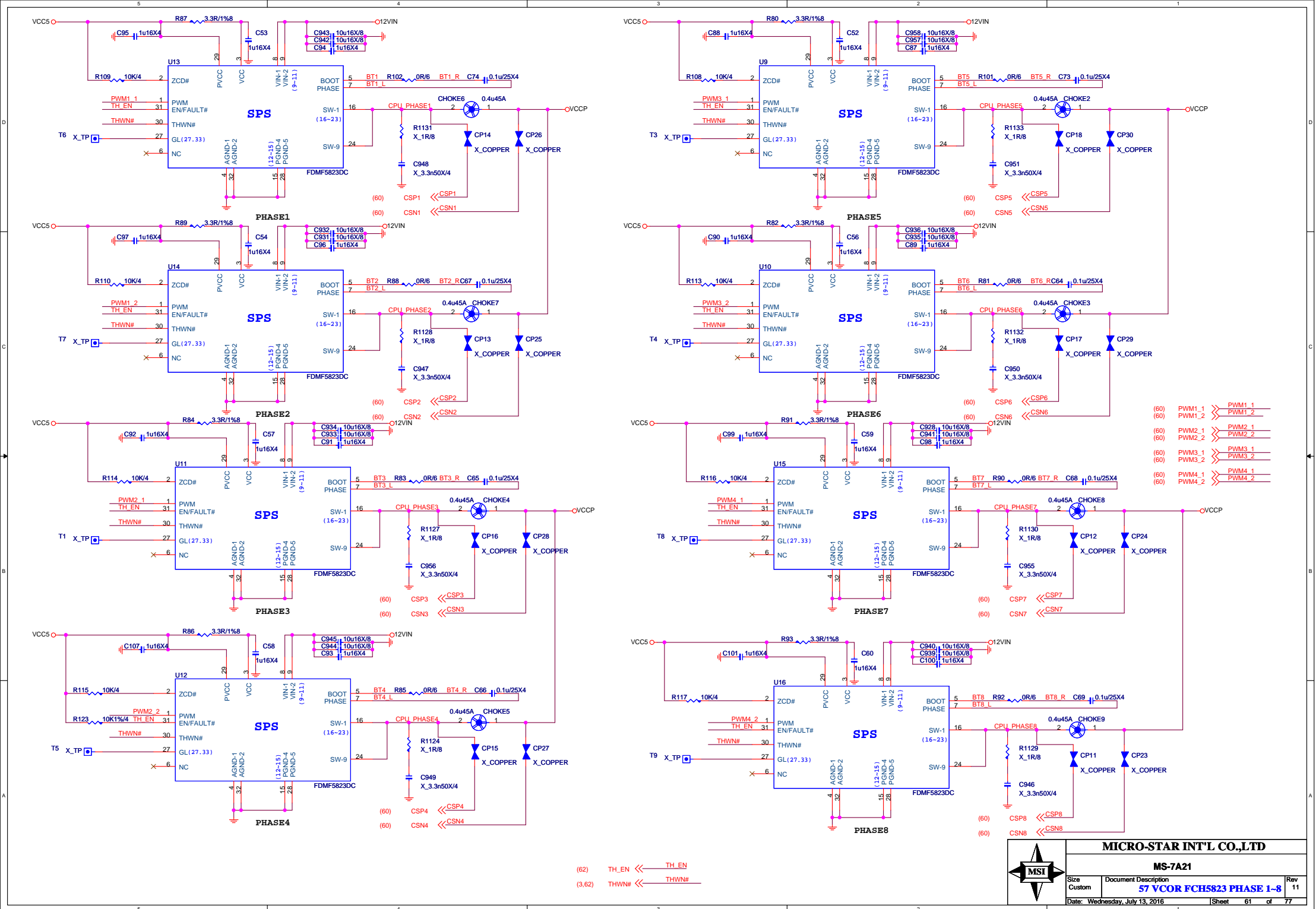


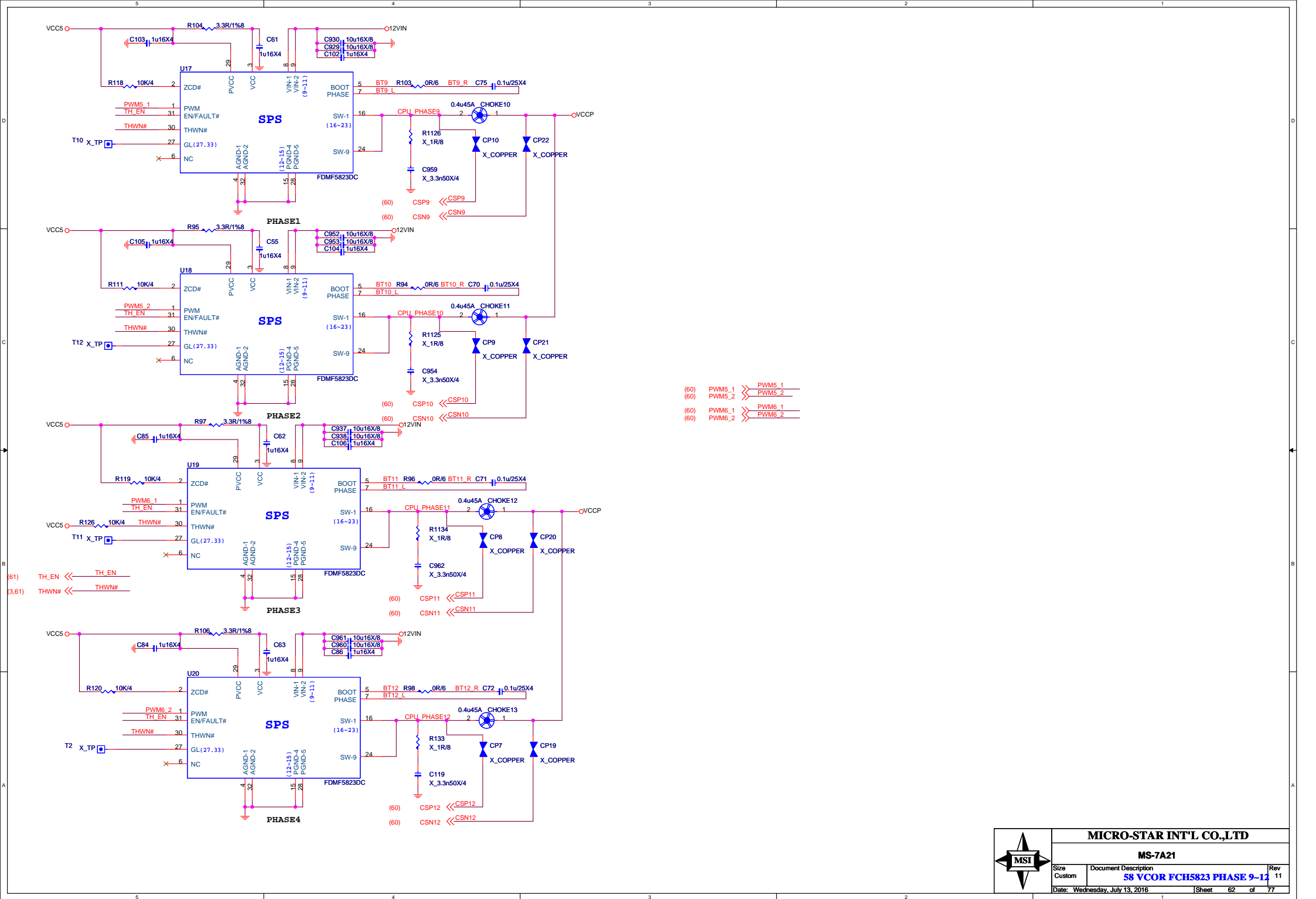


MICRO-STAR INT'L CO.,LTD

MS-7A21

Size Custom	Document Description 56 PHASE DOUBLER 6617	Rev 11
Date: Wednesday, July 13, 2016		Sheet 60 of 77





4DIMM :6A FOR DDR VPP

4DIMM :5A FOR DDR VPP

High: PWM Mode
Low/BZ: PFM Mode

5VDIMM_VPP1

5VDIMM_01

L18 30L3A-15_0805-RH

L19 30L3A-15_0805-RH

5VDIMM_VPP1

C510 22u6.3X/8

C500 22u6.3X/8

C499 22u6.3X/8

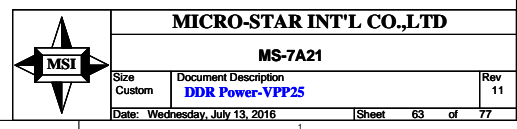
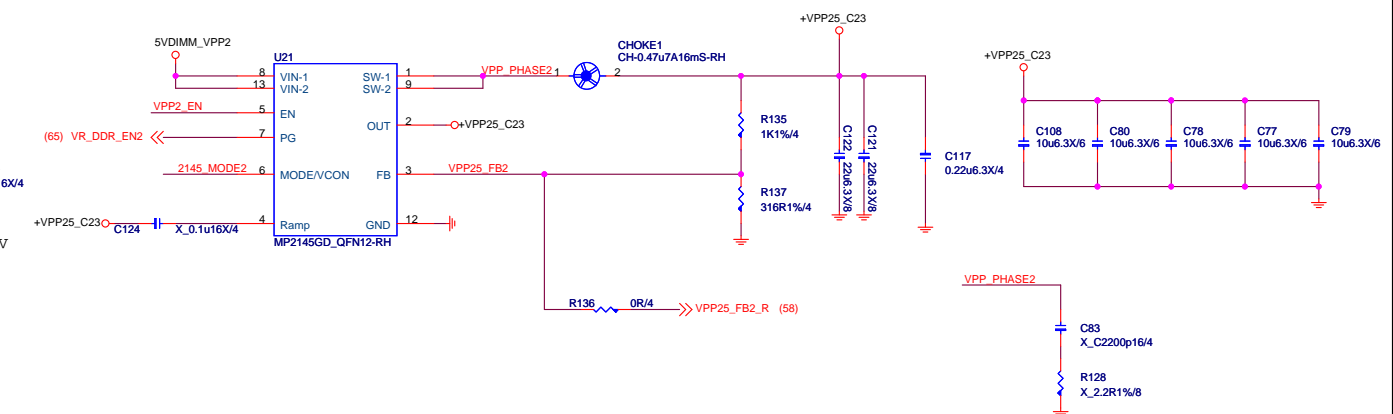
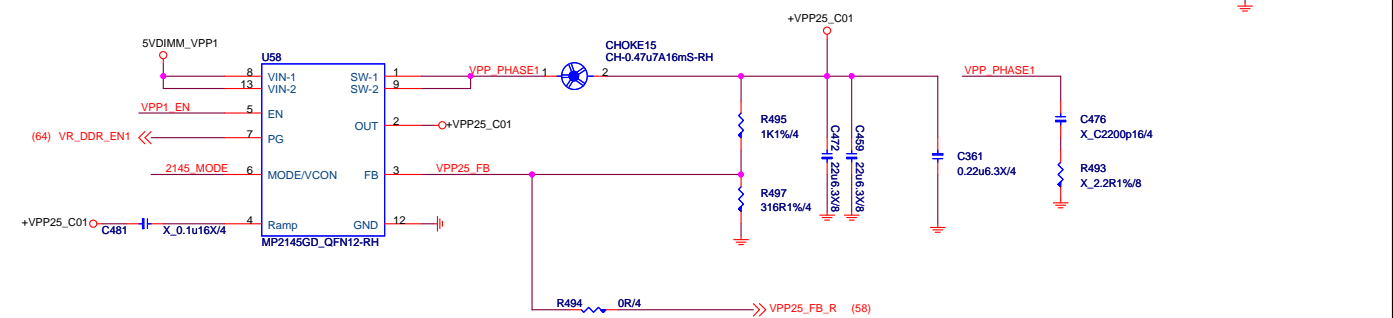
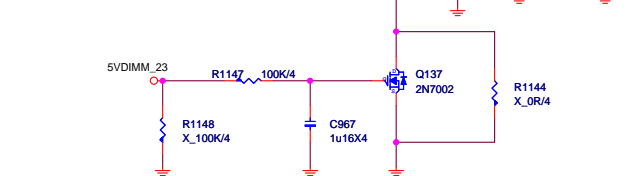
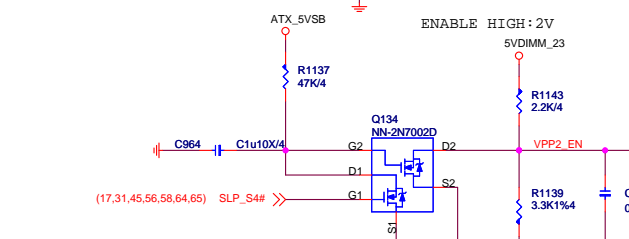
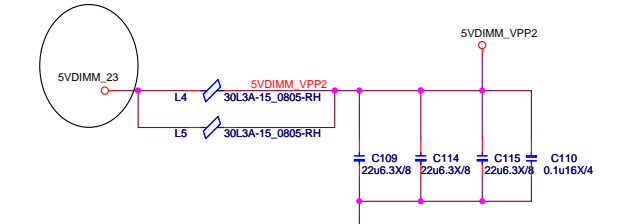
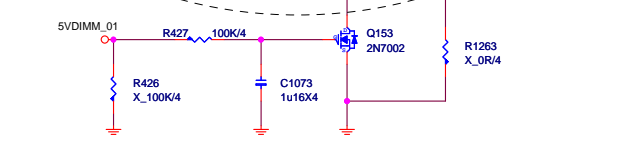
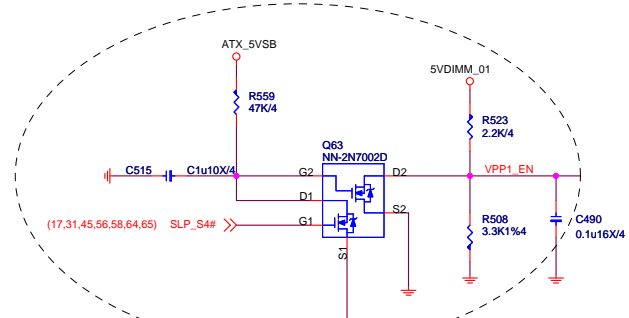
C492 0.1u16X/8

R517 10K/4

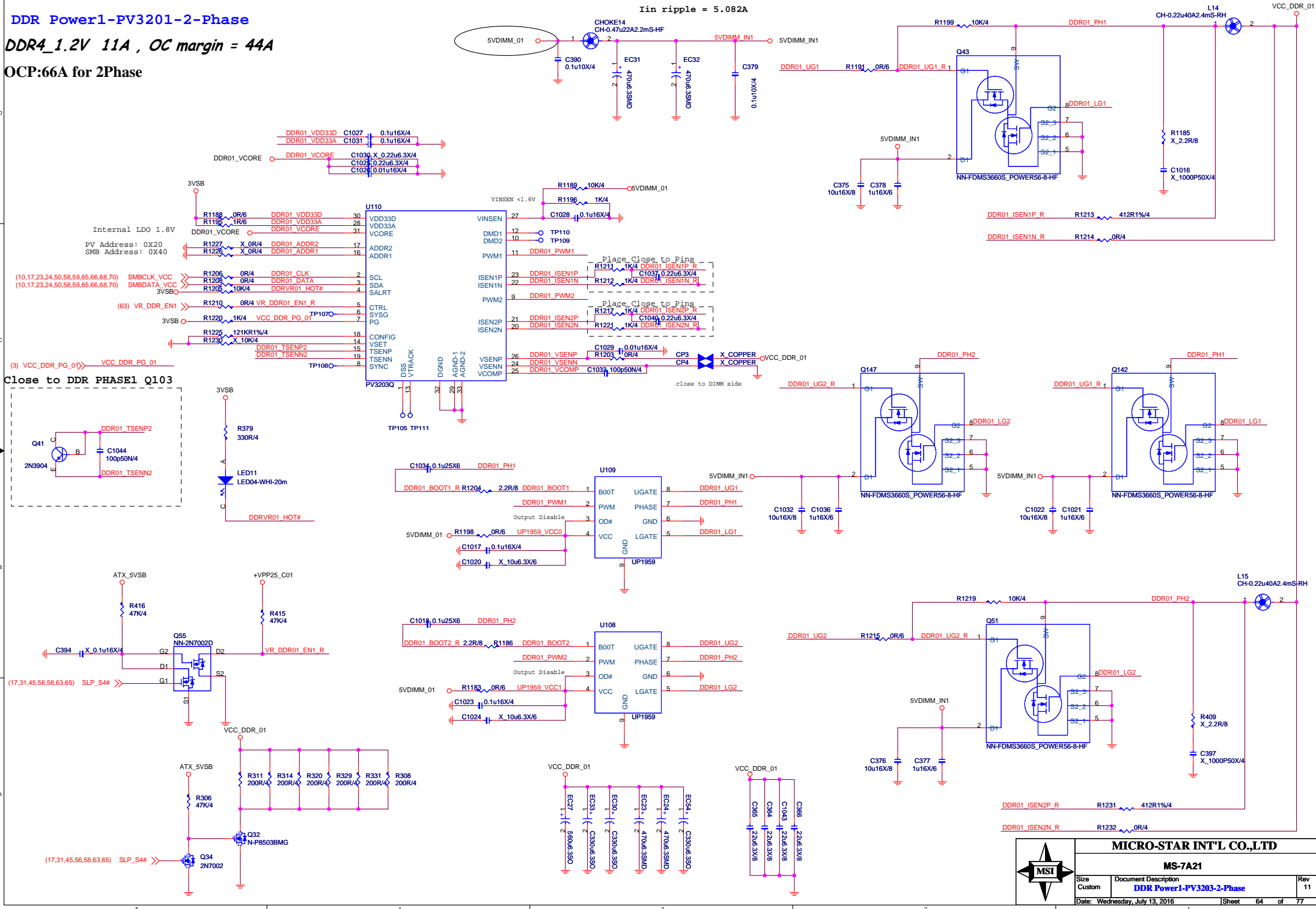
2145_MODE

R509 X_10K/4

C495 0.1u16X/4



OCP:66A for 2Phase



OCP:22A for 2Phase

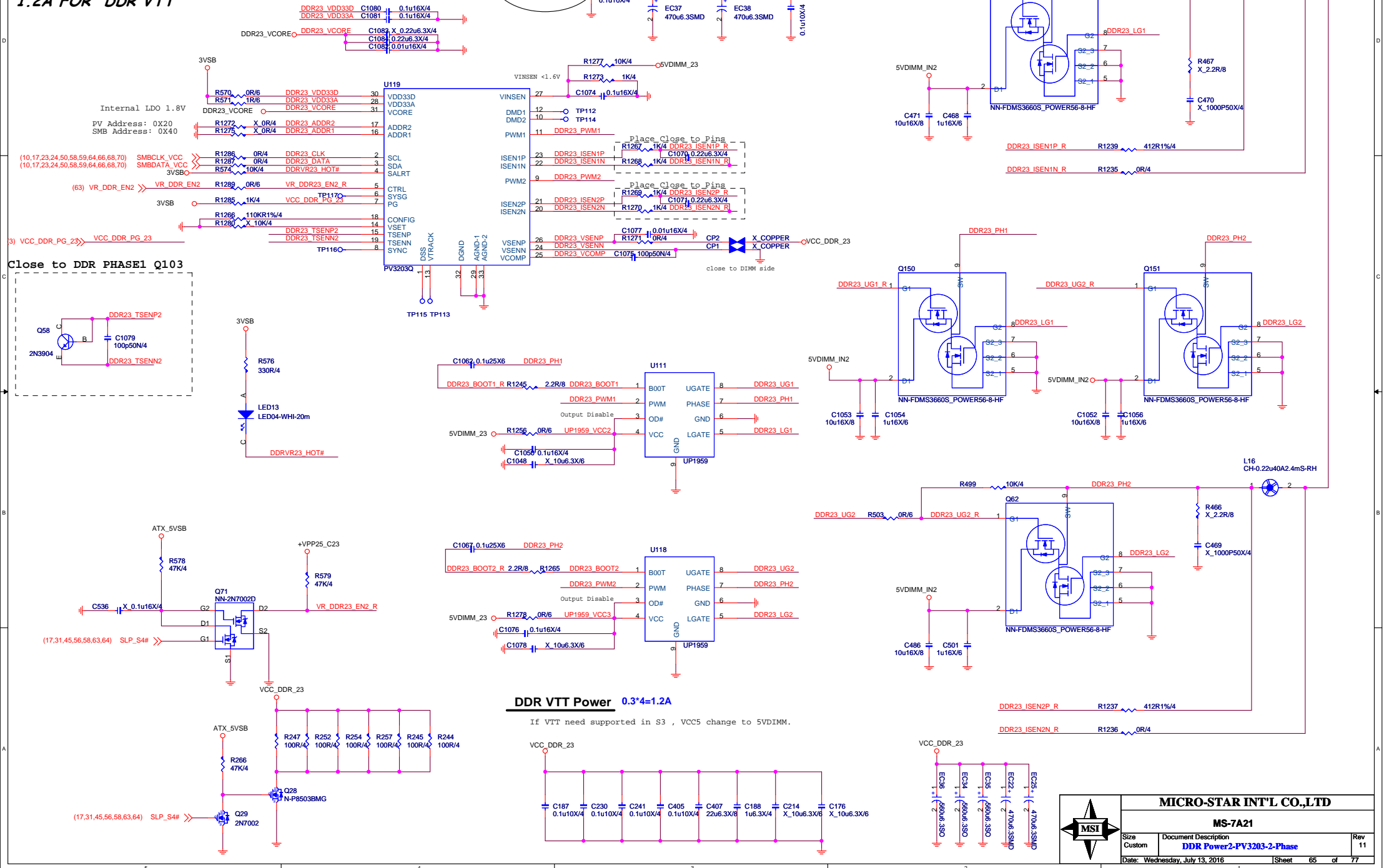
6A FOR 4DIMM

1.2A FOR DDR VTT

Iin ripple = 5.082A

$I_{max}: 20.75A$

Iout ripple = 9A

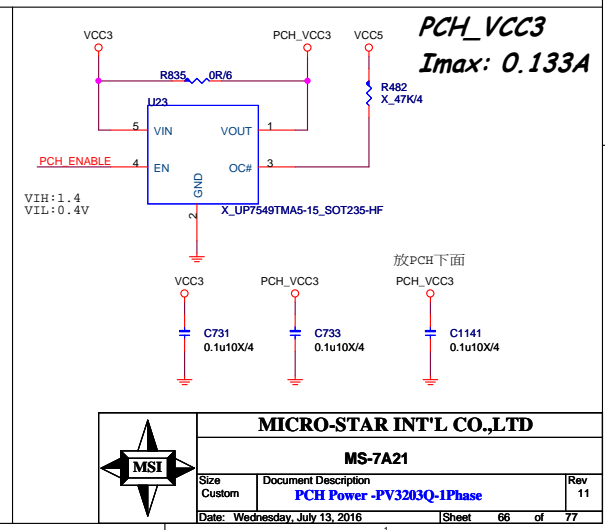
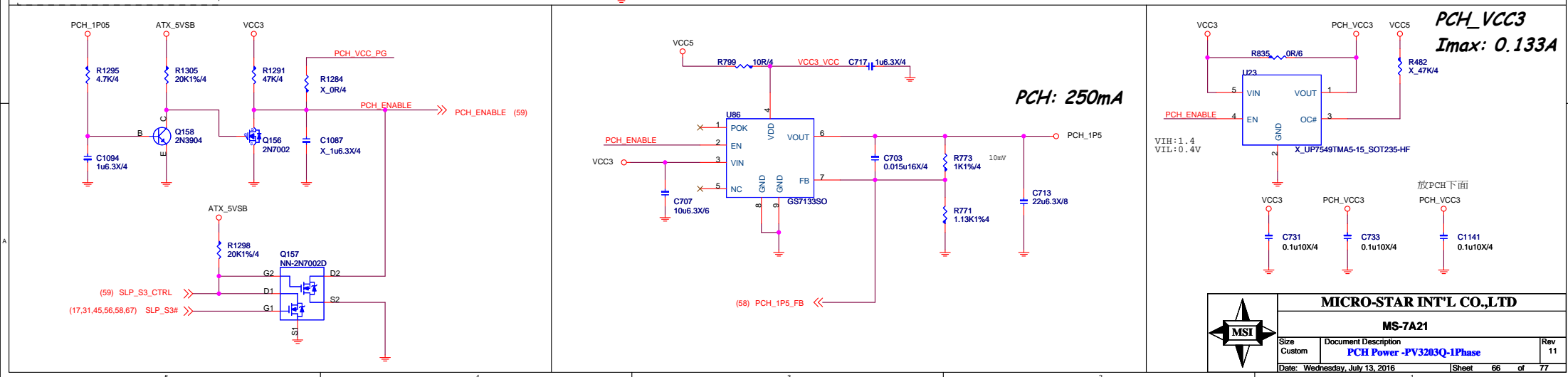


MICRO-STAR INT'L CO.,LTD

MS-7A21

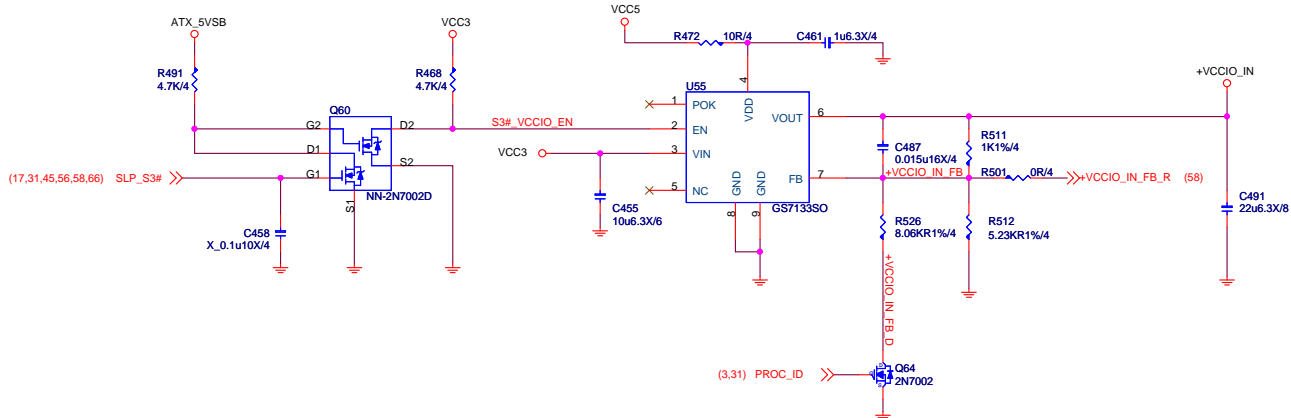
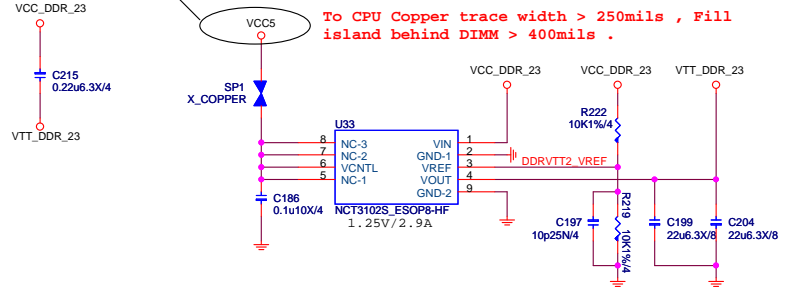
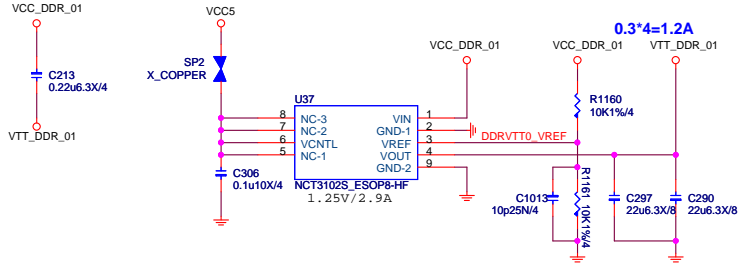
Size Custom	Document Description DDR Power2-PV3203-2-Phase	Rev 11
Date: Wednesday, July 13, 2016		Sheet 65 of 77

PCH Power:1.05V



channel AB

channel CD



PROC_ID	+VCCIO_IN
0	0.95V
1	1.05V

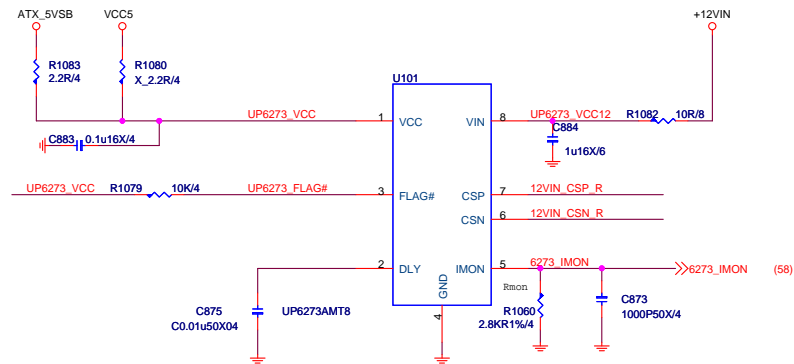


MICRO-STAR INT'L CO.,LTD

MS-7A21

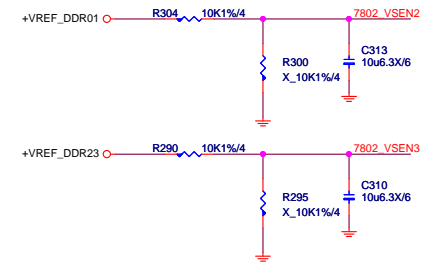
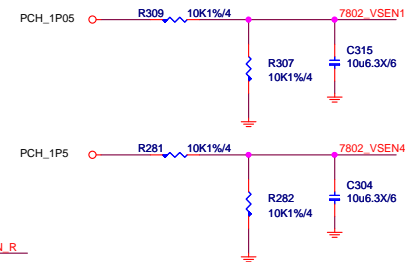
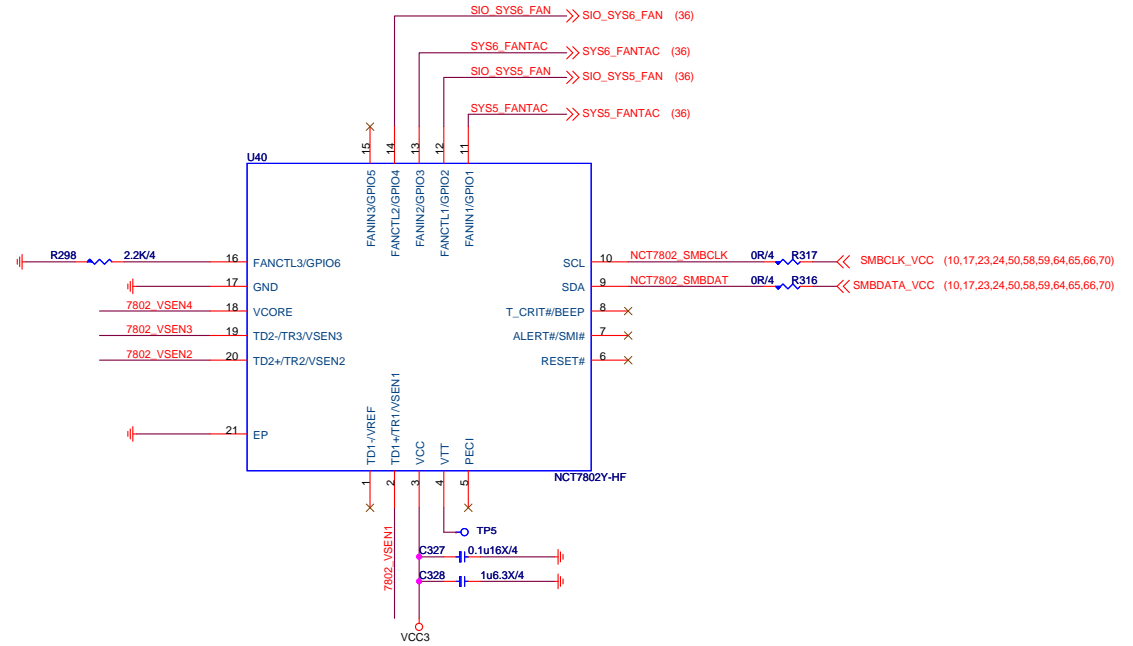
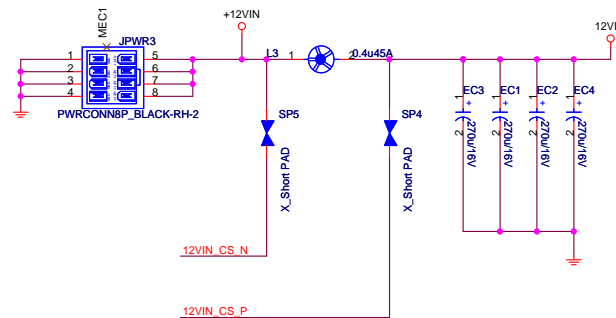
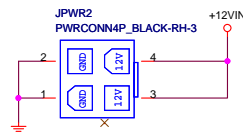
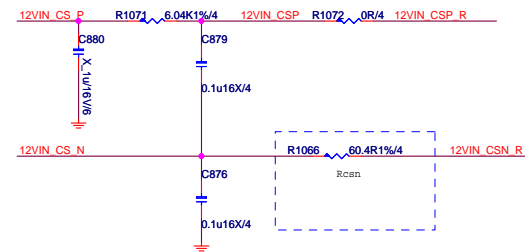
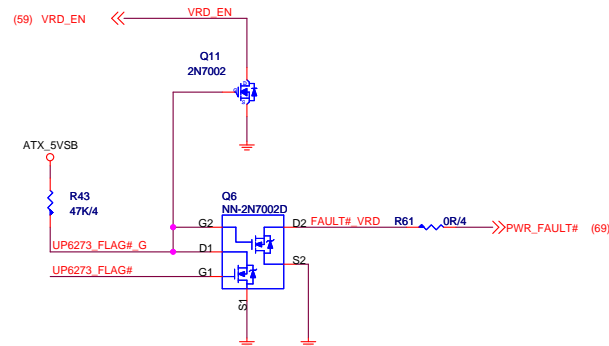
Size Custom	Document Description CLK GEN4105	Rev 11
Date: Wednesday, July 13, 2016		Sheet 67 of 77

POWER METER
OCP: 120A



```
Iin=(Vmon*Rcsn)/(Rmon*Rdc)
Vmon=1.2
can change OCP trigger level by Rcsn and Rmon
```

$$(1.2 * 0.2) / (10K * 0.3m) = 80A$$



UPI VOLTAGE CONSOLE

0xD4: RL=10K												
ADDRESS	0xD4			0xD6			0xD8			0xDA		
	Min	Typ.	Max	Min	Typ.	Max	Min	Typ.	Max	Min	Typ.	Max
BUS_SEL V1otag	0	90	110	170	210	250	310	380	450	510	600	690

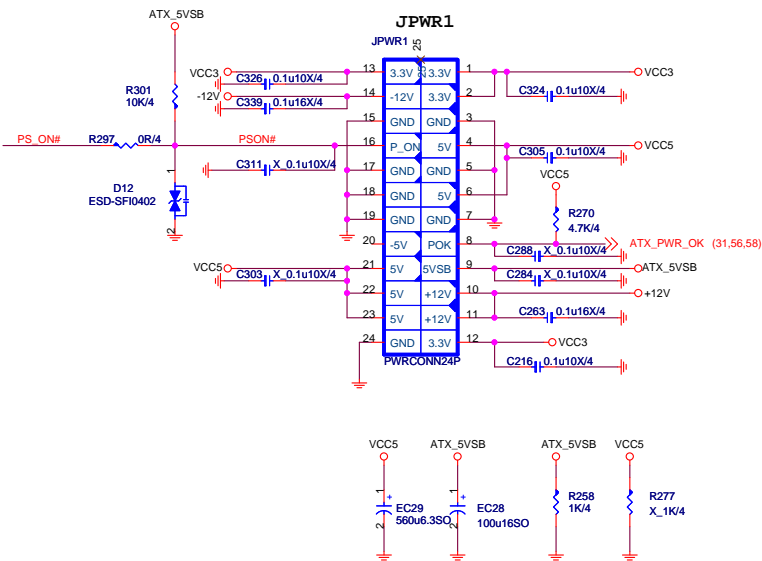


MICRO-STAR INT'L CO.,LTD

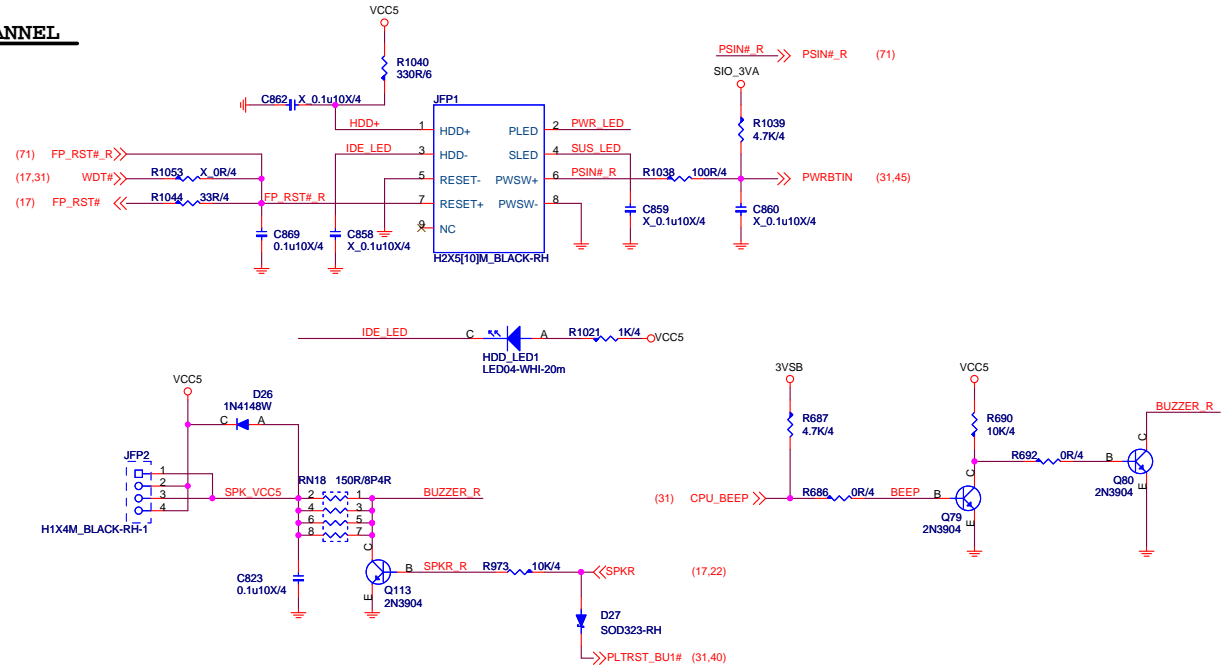
MS-7A21

Size Custom	Document Description CURRENT and VOLTAGE SENSE	Rev 11
Date: Wednesday, July 13, 2016		Sheet 68 of 77

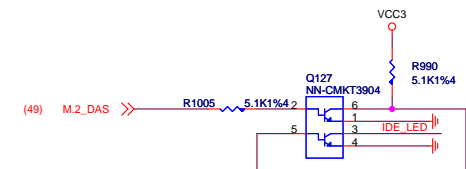
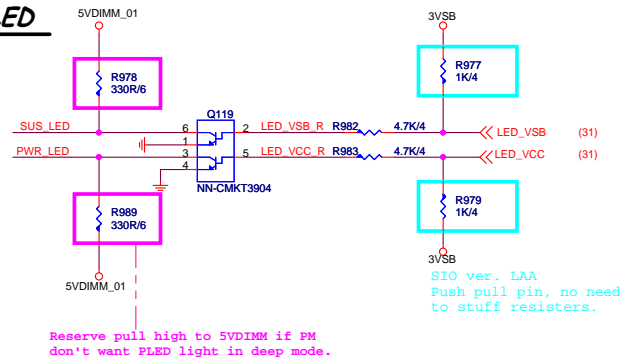
ATX POWER CONNECTOR



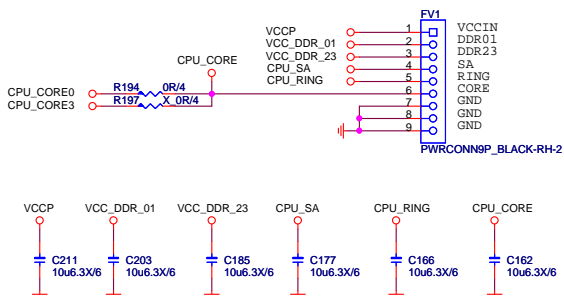
FRONT PANNEL



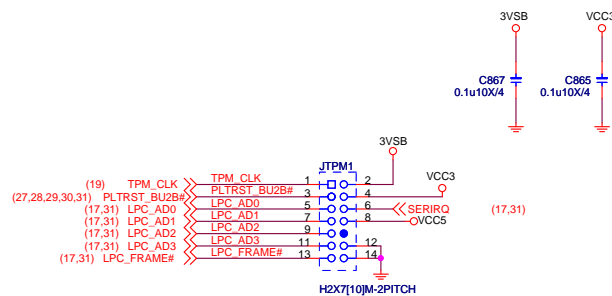
Front Panel LED

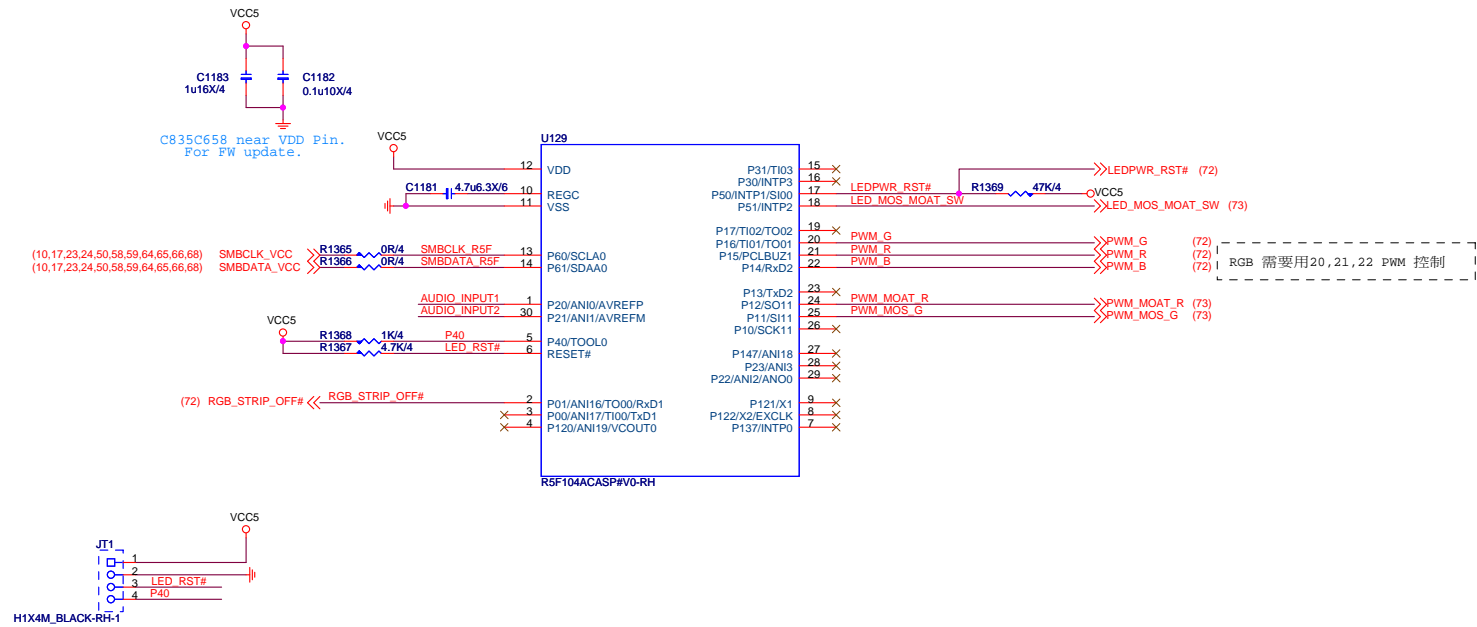


Voltage test point

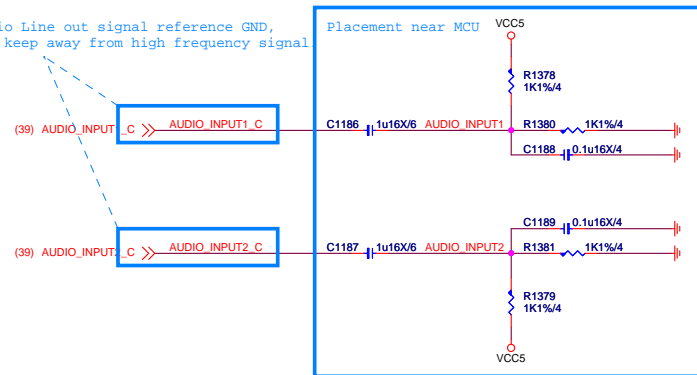


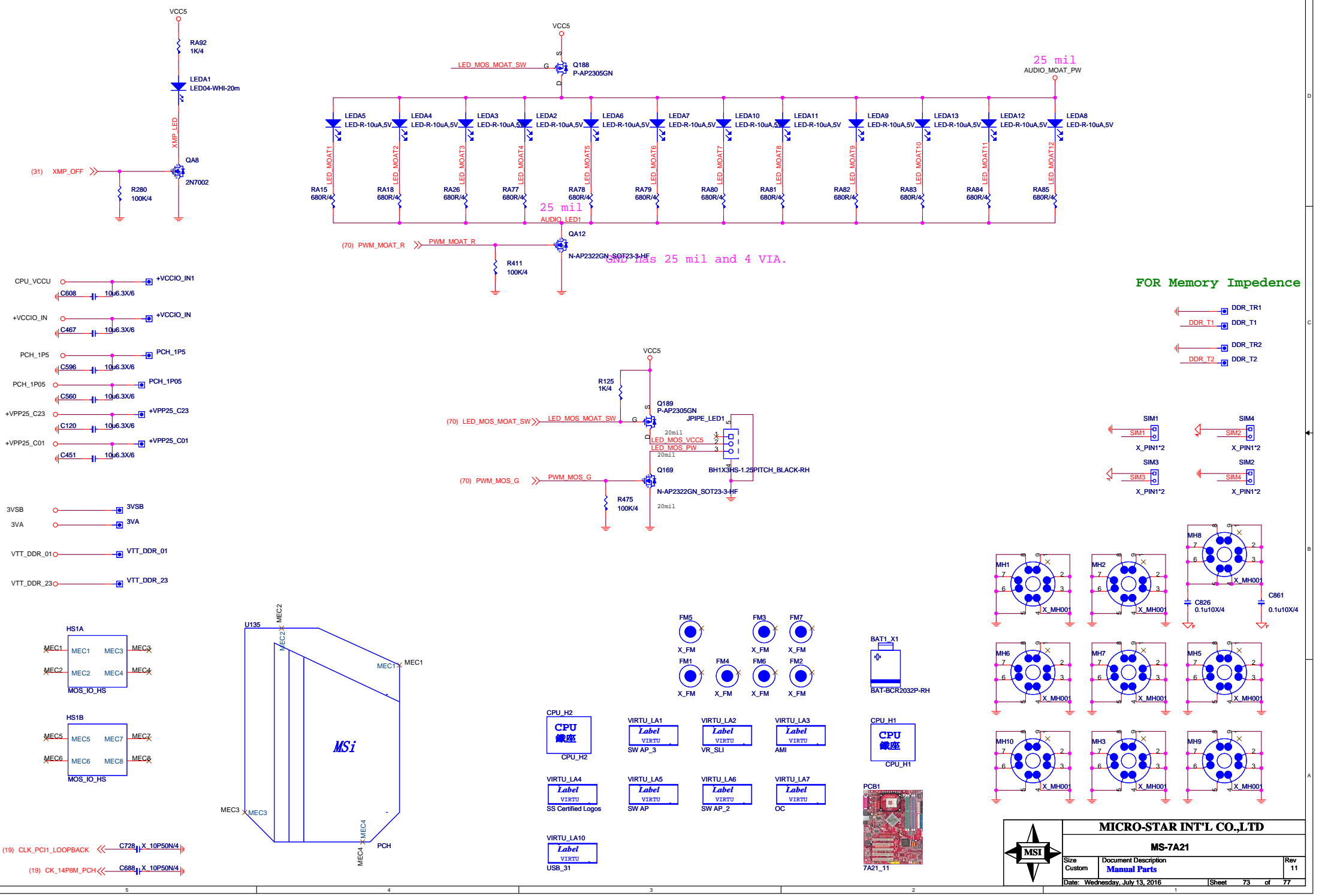
TPM



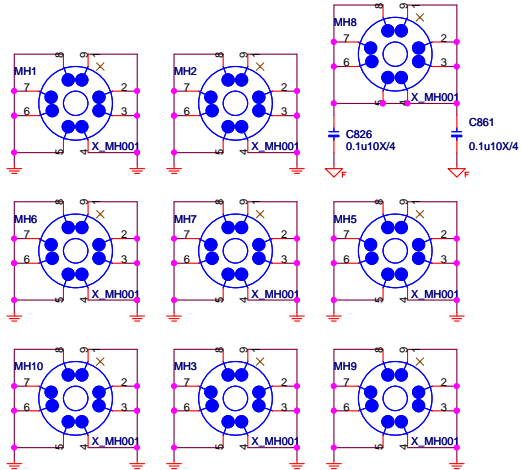
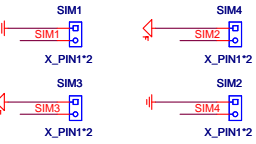
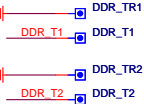


Audio Line out signal reference GND,
and keep away from high frequency signal





FOR Memory Impedence



MICRO-STAR INT'L CO.,LTD			
MS-7A21			
Size	Document Description	Rev	
Custom	Manual Parts	11	
Date: Wednesday, July 13, 2016		Sheet	73 of 77